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STIC Search Report
EIC 2600

STIC Database Tracking Number: 135034

TO: Brian Le **Location: PK1 4B 40** **Art Unit : 2623** **Friday, October 15, 2004** **Case Serial Number: 09977238**	**From: Samir Patel** **Location: EIC 2600** **PK2-3C03** **Phone: 306-0254** **Samir.patel@uspto.gov**

Search Notes

Dear Examiner

Please find attached the search results for 09/977238. I have used the search strategy as per our discussion. I searched the standard Dialog files, IEEE and the internet.

If you would like a re-focus please let me know.

Thank you

Samir Patel

L Number	Hits	Search Text	DB	Time stamp
1	9401	382/145,194.ccls. 438/207,208,231,232,14,16,253,396.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/21 12:22
2	9607	382/145,147,194.ccls. 438/207,208,231,232,14,16,253,396.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/21 12:25
3	2905	HSG or (grow near4 hemispherical near4 grains)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/21 12:25
4	499	(382/145,147,194.ccls. 438/207,208,231,232,14,16,253,396.ccls.) and (HSG or (grow near4 hemispherical near4 grains))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/21 12:25
5	626	(HSG or (grow$3 near4 hemispherical near4 grains) or ((grain or size or degree or volume or dimension) near5 grow$3)) and ((compar$3 or analy$4) same image same pixel)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/21 12:26
6	9	(382/145,147,194.ccls. 438/207,208,231,232,14,16,253,396.ccls.) and ((HSG or (grow$3 near4 hemispherical near4 grains) or ((grain or size or degree or volume or dimension) near5 grow$3)) and ((compar$3 or analy$4) same image same pixel))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/21 12:26
7	190	(semiconductor or wafer) and (HSG or (grow$3 near4 hemispherical near4 grains) or ((grain or size or degree or volume or dimension) near5 grow$3)) and ((compar$3 or analy$4) same (image or pixel or picture) same (predetermine or threshold or limit))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/21 12:26
8	4	(382/145,147,194.ccls. 438/207,208,231,232,14,16,253,396.ccls.) and ((semiconductor or wafer) and (HSG or (grow$3 near4 hemispherical near4 grains) or ((grain or size or degree or volume or dimension) near5 grow$3)) and ((compar$3 or analy$4) same (image or pixel or picture) same (predetermine or threshold or limit)))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/21 12:26

S12879 U USPT sem and semiconductor$2 and target$2 and image near file$2 and (growth or height or thick$4) — 2004-10-14 14:28:56

☐ 1. Document ID: US 6801650 B1

L2: Entry 1 of 23 File: USPT Oct 5, 2004

US-PAT-NO: 6801650
DOCUMENT-IDENTIFIER: US 6801650 B1

TITLE: Mechanism and method for controlling focal point position of UV light and apparatus and method for inspection

DATE-ISSUED: October 5, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kikuchi; Hiroki	Kanagawa			JP
Nogami; Asahiko	Tokyo			JP
Morita; Masayuki	Saitama			JP

US-CL-CURRENT: 382/145; 250/201.4, 250/372, 250/548

Full | Title | Citation | Front | Review | Classification | Date | Reference

Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 6785873 B1

L2: Entry 2 of 23 File: USPT Aug 31, 2004

US-PAT-NO: 6785873
DOCUMENT-IDENTIFIER: US 6785873 B1

TITLE: Emulation system with multiple asynchronous clocks

DATE-ISSUED: August 31, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tseng; Ping-Sheng	Sunnyvale	CA		

US-CL-CURRENT: 716/4; 716/1

☐ 3. Document ID: US 6777677 B2

L2: Entry 3 of 23 File: USPT Aug 17, 2004

US-PAT-NO: 6777677
DOCUMENT-IDENTIFIER: US 6777677 B2

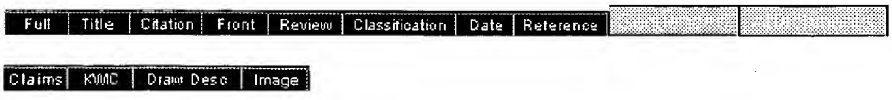
TITLE: Method of inspecting pattern and inspecting instrument

DATE-ISSUED: August 17, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nozoe; Mari	Hino			JP
Nishiyama; Hidetoshi	Kokubunji			JP
Hijikata; Shigeaki	Ome			JP
Watanabe; Kenji	Ome			JP
Abe; Koji	Hitachinaka			JP

US-CL-CURRENT: 250/310; 250/307



☐ 4. Document ID: US 6759655 B2

L2: Entry 4 of 23 File: USPT Jul 6, 2004

US-PAT-NO: 6759655
DOCUMENT-IDENTIFIER: US 6759655 B2

TITLE: Inspection method, apparatus and system for circuit pattern

DATE-ISSUED: July 6, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nara; Yasuhiko	Hitachinaka			JP
Machida; Kazuhisa	Kawasaki			JP
Nozoe; Mari	Hino			JP
Morioka; Hiroshi	Higashimurayama			JP
Usami; Yasutsugu	Hitachinaka			JP
Hiroi; Takashi	Yokohama			JP
Hayakawa; Kohichi	Hitachinaka			JP

US-CL-CURRENT: 250/310; 250/307

☐ 5. Document ID: US 6757645 B2

L2: Entry 5 of 23 File: USPT Jun 29, 2004

US-PAT-NO: 6757645
DOCUMENT-IDENTIFIER: US 6757645 B2

TITLE: Visual inspection and verification system

DATE-ISSUED: June 29, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chang; Fang-Cheng	Mountain View	CA		
Wang; Yao-Ting	Sunnyvale	CA		
Pati; Yagyensh C.	Redwood City	CA		
Karklin; Linard N.	Sunnyvale	CA		

US-CL-CURRENT: 703/13; 716/19, 716/21

☐ 6. Document ID: US 6757621 B2

L2: Entry 6 of 23 File: USPT Jun 29, 2004

US-PAT-NO: 6757621
DOCUMENT-IDENTIFIER: US 6757621 B2

TITLE: Process management system

DATE-ISSUED: June 29, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mizuno; Fumio	Tokorozawa			JP
Isogai; Seiji	Hitachinaka			JP
Watanabe; Kenji	Oume			JP
Yoshitake; Yasuhiro	Yokosuka			JP
Asakawa; Terushige	Hamura			JP

Ohyama; Yuichi	Isezaki	JP
Sugimoto; Hidekuni	Honjyo	JP
Ishikawa; Seiji	Kawasaki	JP
Shiba; Masataka	Yokohama	JP
Nakazato; Jun	Shinagawa-ku	JP
Ariga; Makoto	Yokohama	JP
Yokouchi; Tetsuji	Yokohama	JP
Hamada; Toshimitsu	Yokohama	JP
Suzuki; Ikuo	Hitachinaka	JP
Ikota; Masami	Higashiyamato	JP
Nozoe; Mari	Oume	JP
Miyazaki; Isao	Isezaki	JP
Shigyo; Yoshiharu	Takasaki	JP

US-CL-CURRENT: 702/35; 257/E21.525, 700/121, 702/36, 702/40

☐ 7. Document ID: US 6754763 B2

L2: Entry 7 of 23 File: USPT Jun 22, 2004

US-PAT-NO: 6754763
DOCUMENT-IDENTIFIER: US 6754763 B2

TITLE: Multi-board connection system for use in electronic design automation

DATE-ISSUED: June 22, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lin; Sharon Sheau-Pyng	Cupertino	CA		

US-CL-CURRENT: 710/317; 361/748, 370/257, 710/305, 712/33

☐ 8. Document ID: US 6651225 B1

L2: Entry 8 of 23 File: USPT Nov 18, 2003

US-PAT-NO: 6651225
DOCUMENT-IDENTIFIER: US 6651225 B1

TITLE: Dynamic evaluation logic system and method

DATE-ISSUED: November 18, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lin; Sharon Sheau-Pyng	Cupertino	CA		
Tseng; Ping-Sheng	Sunnyvale	CA		
Chang; Chwen-Cher	Fremont	CA		
Hwang; Su-Jen	Los Altos	CA		

US-CL-CURRENT: 716/4; 716/1

☐ 9. Document ID: US 6583414 B2

L2: Entry 9 of 23 File: USPT Jun 24, 2003

US-PAT-NO: 6583414
DOCUMENT-IDENTIFIER: US 6583414 B2

TITLE: Method of inspecting pattern and inspecting instrument

DATE-ISSUED: June 24, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nozoe; Mari	Hino			JP
Nishiyama; Hidetoshi	Kokubunji			JP
Hijikata; Shigeaki	Ome			JP
Watanabe; Kenji	Ome			JP
Abe; Koji	Hitachinaka			JP

US-CL-CURRENT: 250/310; 250/397

☐ 10. Document ID: US 6578188 B1

L2: Entry 10 of 23 File: USPT Jun 10, 2003

US-PAT-NO: 6578188
DOCUMENT-IDENTIFIER: US 6578188 B1

TITLE: Method and apparatus for a network-based mask defect printability analysis system

DATE-ISSUED: June 10, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY

Pang; Linyong	Stanford	CA
Howard; Daniel William	Santa Clara	CA
Karklin; Linard	Sunnyvale	CA

US-CL-CURRENT: 716/19; 977/DIG.1

☐ 11. Document ID: US 6567168 B2

L2: Entry 11 of 23 File: USPT May 20, 2003

US-PAT-NO: 6567168
DOCUMENT-IDENTIFIER: US 6567168 B2
**** See image for Certificate of Correction ****

TITLE: Inspection method, apparatus and system for circuit pattern

DATE-ISSUED: May 20, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nara; Yasuhiko	Hitachinaka			JP
Hiroi; Takashi	Yokohama			JP

US-CL-CURRENT: 356/394; 250/310

☐ 12. Document ID: US 6542830 B1

L2: Entry 12 of 23 File: USPT Apr 1, 2003

US-PAT-NO: 6542830
DOCUMENT-IDENTIFIER: US 6542830 B1

TITLE: Process control system

DATE-ISSUED: April 1, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mizuno; Fumio	Tokorozawa			JP
Isogai; Seiji	Hitachinaka			JP
Watanabe; Kenji	Oume			JP
Yoshitake; Yasuhiro	Yokosuka			JP
Asakawa; Terushige	Hamura			JP
Ohyama; Yuichi	Isezaki			JP
Sugimoto; Hidekuni	Honjyo			JP
Ishikawa; Seiji	Kawasaki			JP
Shiba; Masataka	Yokohama			JP
Nakazato; Jun	Shinagawa-ku			JP
Ariga; Makoto	Yokohama			JP
Yokouchi; Tetsuji	Yokohama			JP
Hamada; Toshimitsu	Yokohama			JP
Suzuki; Ikuo	Hitachinaka			JP
Ikota; Masami	Higashiyamato			JP
Nozoe; Mari	Oume			JP
Miyazaki; Isao	Isezaki			JP
Shigyo; Yoshiharu	Takasaki			JP

US-CL-CURRENT: 702/35; 257/E21.525, 700/109, 700/110, 700/121, 702/36, 702/40, 702/81, 702/83

☐ 13. Document ID: US 6531697 B1

L2: Entry 13 of 23 File: USPT Mar 11, 2003

US-PAT-NO: 6531697
DOCUMENT-IDENTIFIER: US 6531697 B1

TITLE: Method and apparatus for scanning transmission electron microscopy

DATE-ISSUED: March 11, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nakamura; Kuniyasu	Musashino			JP
Kakibayashi; Hiroshi	Nagareyama			JP
Ichihashi; Mikio	Kodaira			JP
Isakozawa; Shigeto	Hitachinaka			JP
Sato; Yuji	Hitachinaka			JP
Hashimoto; Takahito	Hitachinaka			JP

US-CL-CURRENT: 250/311; 250/302, 250/305, 250/306, 250/310

☐ 14. Document ID: US 6504609 B2

L2: Entry 14 of 23 File: USPT Jan 7, 2003

US-PAT-NO: 6504609
DOCUMENT-IDENTIFIER: US 6504609 B2

TITLE: Inspection method, apparatus and system for circuit pattern

DATE-ISSUED: January 7, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nara; Yasuhiko	Hitachinaka			JP
Machida; Kazuhisa	Kawasaki			JP
Nozoe; Mari	Hino			JP
Morioka; Hiroshi	Higashimurayama			JP
Usami; Yasutsugu	Hitachinaka			JP
Hiroi; Takashi	Yokohama			JP

US-CL-CURRENT: 356/394

☐ 15. Document ID: US 6493082 B2

L2: Entry 15 of 23 File: USPT Dec 10, 2002

US-PAT-NO: 6493082
DOCUMENT-IDENTIFIER: US 6493082 B2

TITLE: Inspection method, apparatus and system for circuit pattern

DATE-ISSUED: December 10, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nara; Yasuhiko	Hitachinaka			JP
Machida; Kazuhisa	Kawasaki			JP
Nozoe; Mari	Hino			JP

Morioka; Hiroshi	Higashimurayama	JP
Usami; Yasutsugu	Hitachinaka	JP
Hiroi; Takashi	Yokohama	JP
Hayakawa; Kohichi	Hitachinaka	JP
Ito; Maki	Koganei	JP

US-CL-CURRENT: 356/394; 382/145

☐ 16. Document ID: US 6480279 B2

L2: Entry 16 of 23 File: USPT Nov 12, 2002

US-PAT-NO: 6480279
DOCUMENT-IDENTIFIER: US 6480279 B2

TITLE: Inspection method, apparatus and system for circuit pattern

DATE-ISSUED: November 12, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nara; Yasuhiko	Hitachinaka			JP
Machida; Kazuhisa	Kawasaki			JP
Nozoe; Mari	Hino			JP
Morioka; Hiroshi	Higashimurayama			JP
Usami; Yasutsugu	Hitachinaka			JP
Hiroi; Takashi	Yokahama			JP

US-CL-CURRENT: 356/394; 382/145

Full | Title | Citation | Front | Review | Classification | Date | Reference

Claims | KWIC | Draw Desc | Image

☐ 17. Document ID: US 6476913 B1

L2: Entry 17 of 23 File: USPT Nov 5, 2002

US-PAT-NO: 6476913
DOCUMENT-IDENTIFIER: US 6476913 B1
**** See image for Certificate of Correction ****

TITLE: Inspection method, apparatus and system for circuit pattern

DATE-ISSUED: November 5, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Machida; Kazuhisa	Kawasaki			JP
Nozoe; Mari	Hino			JP
Morioka; Hiroshi	Higashimurayama			JP
Usami; Yasutsugu	Hitachinaka			JP
Hiroi; Takashi	Yokohama			JP
Ito; Maki	Koganei			JP

US-CL-CURRENT: 356/394

Full | Title | Citation | Front | Review | Classification | Date | Reference

Claims | KWIC | Draw Desc | Image

☐ 18. Document ID: US 6421251 B1

L2: Entry 18 of 23 File: USPT Jul 16, 2002

US-PAT-NO: 6421251
DOCUMENT-IDENTIFIER: US 6421251 B1
**** See image for Certificate of Correction ****

TITLE: Array board interconnect system and method

DATE-ISSUED: July 16, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lin; Sharon Sheau-Pyng	Cupertino	CA	95014	

US-CL-CURRENT: 361/788; 361/803

☐ 19. Document ID: US 6421122 B2

L2: Entry 19 of 23 File: USPT Jul 16, 2002

US-PAT-NO: 6421122
DOCUMENT-IDENTIFIER: US 6421122 B2
**** See image for Certificate of Correction ****

TITLE: Inspection method, apparatus and system for circuit pattern

DATE-ISSUED: July 16, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nara; Yasuhiko	Hitachinaka			JP
Machida; Kazuhisa	Kawasaki			JP

Nozoe; Mari	Hino	JP
Morioka; Hiroshi	Higashimurayama	JP
Usami; Yasutsugu	Hitachinaka	JP
Hiroi; Takashi	Yokohama	JP
Hayakawa; Kohichi	Hitachinaka	JP
Ito; Maki	Koganei	JP

US-CL-CURRENT: 356/394; 382/145

Full | Title | Citation | Front | Review | Classification | Date | Reference

Claims | KWIC | Draw Desc | Image

☐ 20. Document ID: US 6389379 B1

L2: Entry 20 of 23 File: USPT May 14, 2002

US-PAT-NO: 6389379
DOCUMENT-IDENTIFIER: US 6389379 B1

TITLE: Converification system and method

DATE-ISSUED: May 14, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lin; Sharon Sheau-Pyng	Cupertino	CA		
Tseng; Ping-Sheng	Sunnyvale	CA		

US-CL-CURRENT: 703/14; 703/23, 716/5

Full | Title | Citation | Front | Review | Classification | Date | Reference

Claims | KWIC | Draw Desc | Image

21. Document ID: US 6388747 B2

L2: Entry 21 of 23 File: USPT May 14, 2002

US-PAT-NO: 6388747
DOCUMENT-IDENTIFIER: US 6388747 B2

TITLE: Inspection method, apparatus and system for circuit pattern

DATE-ISSUED: May 14, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nara; Yasuhiko	Hitachinaka			JP
Machida; Kazuhisa	Kawasaki			JP
Nozoe; Mari	Hino			JP
Morioka; Hiroshi	Higashimurayama			JP
Usami; Yasutsugu	Hitachinaka			JP
Hiroi; Takashi	Yokohama			JP

US-CL-CURRENT: 356/394

☐ 22. Document ID: US 6321366 B1

L2: Entry 22 of 23 File: USPT Nov 20, 2001

US-PAT-NO: 6321366
DOCUMENT-IDENTIFIER: US 6321366 B1

TITLE: Timing-insensitive glitch-free logic system and method

DATE-ISSUED: November 20, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tseng; Ping-Sheng	Sunnyvale	CA		
Lin; Sharon Sheau-Ping	Cupertino	CA		
Shen; Quincy Kun-Hsu	Union City	CA		

US-CL-CURRENT: 716/6; 703/19

☐ 23. Document ID: US 5777327 A

L2: Entry 23 of 23 File: USPT Jul 7, 1998

US-PAT-NO: 5777327
DOCUMENT-IDENTIFIER: US 5777327 A

TITLE: Pattern shape inspection apparatus for forming specimen image on display apparatus

DATE-ISSUED: July 7, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mizuno; Fumio	Tokorozawa			JP

US-CL-CURRENT: 250/310; 250/306

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File 344:Chinese Patents Abs Aug 1985-2004/May
         (c) 2004 European Patent Office
File 347:JAPIO Nov 1976-2004/Jun(Updated 041004)
         (c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200465
         (c) 2004  Thomson Derwent

Set     Items   Description
S1    3428524   SEMICONDUCTOR?? OR WAFER?? OR CIRCUIT?? OR IC OR INTEGRAT?-
               ??(2N)CIRCUIT?? OR CHIP?? OR SEMI()CONDUCT????
S2      69221   (SIZE?? OR DEGREE?? OR AMOUNT?? OR VOLUME?? OR DIMENSION??
               OR HEIGHT?? OR GROW??? OR WIDT?? OR INTENSITY?? OR DENSIT??)(-
               5N)(HSG OR HSGS OR (HEMISPHERICAL??()GRAIN??) OR GRAIN??)
S3     149466   PIXEL?? OR PEL OR (PICTURE??()ELEMENT??) OR SUB()PIX?? OR -
               SUBPIXEL??
S4       7451   (THRESHOLD?? OR PREDETERMIN??? OR LIMIT??)(5N)S3
S5    1707461   IMAGE?? OR PHOTOGRAPH?? OR PICTURE? ? OR PHOTO??
S6       1914   RATIO??(5N)(PIXEL?? OR PEL OR (PICTURE??()ELEMENT??) OR SU-
               B()PIX?? OR SUBPIXEL??)
S7       2787   SEM OR SCANNING??(3N)MICROSCOPY??
S8      74750   AU=(JUN C? OR JUN, C? OR CHON S? OR CHON, S? OR CHOI S? OR
               CHOI, S? OR KIM K? OR KIM, K? OR LEE S? OR LEE, S? OR YANG Y?
               OR YANG, Y? OR KIM S? OR KIM, S?)
S9       5293   S1 AND S2
S10         0   S9 AND S4 AND S5
S11         0   S9 AND S4
S12        42   S9 AND S3
S13         1   S12 AND S6
S14         0   S13 AND S7
S15      1069   S1 AND S7
S16         1   S12 AND S7
S17         1   S16 NOT S13
S18        21   S15 AND S3
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S20        12   S19 NOT AD=20001019:20041014/PR
S21     12340   S8 AND S1
S22        32   S21 AND S2
S23         0   S22 AND S4 AND S5
S24         0   S22 AND S4
S25         1   S22 AND S3
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13/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014768775 **Image available**
WPI Acc No: 2002-589479/200263
XRPX Acc No: N02-467729

Grain growth degree **analysis method for** semiconductor wafer , **involves calculating** ratio **of** pixels **whose standardized values exceed preset value, to that of total** pixels **in target zone of image file of** wafer

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU); CHOI S (CHOI-I); CHON S (CHON-I); JUN C (JUNC-I); KIM K (KIMK-I); KIM S (KIMS-I); LEE S (LEES-I); YANG Y (YANG-I)
Inventor: CHOI S; CHON S; JUN C; KIM K; KIM S; LEE S; YANG Y; CHOI S B; JUN C S; JUN S M; KIM G W; KIM S M; LEE S G; LEE S H; YANG Y S; JEON C S; JEON S M

Number of Countries: 005 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020072133	A1	20020613	US 2001977238	A	20011016	200263 B
JP 2002228607	A	20020814	JP 2001313076	A	20011010	200268
KR 2002030674	A	20020425	KR 200061717	A	20001019	200269
KR 347764	B	20020809	KR 200061717	A	20001019	200311
DE 10151396	A1	20030508	DE 1051396	A	20011018	200331
TW 521363	A	20030221	TW 2001119055	A	20010803	200364

Priority Applications (No Type Date): KR 200061717 A 20001019
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020072133	A1		29	H01L-021/66	
JP 2002228607	A		16	G01N-023/225	
KR 2002030674	A			H01L-021/66	
KR 347764	B			H01L-021/66	Previous Publ. patent KR 2002030674
DE 10151396	A1			H01L-021/66	
TW 521363	A			H01L-021/66	

Grain growth degree **analysis method for** semiconductor wafer , **involves calculating** ratio **of** pixels **whose standardized values exceed preset value, to that of total** pixels **in target zone of image file of** wafer

Abstract (Basic):
... is selected from an image file generated by scanning a specific surface portion of a **semiconductor wafer** (30). An image data of the **pixels** in the target zone are standardized and compared with a preset threshold value. The **grain growth degree** is determined by obtaining a **ratio** of **pixels** whose image values exceed the preset value, to that of the total **pixels** in the zone.
... An INDEPENDENT CLAIM is included for **grain growth degree** analysis apparatus...

...For analyzing **grain growth degree** in **semiconductor wafer** .
...

...Analyzes the distribution degree of unevenness with respect to the surface of the **wafer** . Determines **grain growth** rate accurately and rapidly. Increases productivity by reducing analysis time and by improving quality of...

...The figure shows an exploded schematic view of the **grain growth degree** analysis apparatus...

... **Semiconductor wafer** (30
...Title Terms: **SEMICONDUCTOR** ;

17/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004002054
WPI Acc No: 1984-147596/198424
XRPX Acc No: N84-109740
Automatic object dimension measuring appts. - has scanning electron microscope with dimension measuring section and is for metal crystal, sub- grain **boundary, powder particle** size
Patent Assignee: TOKYO SHIBAURA DENKI KK (TOKE)
Inventor: KANO M; NAKAO S; OKUMURA K; YAMAJI H
Number of Countries: 005 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 110301	A	19840613	EP 83111669	A	19831122	198424	B
US 4567364	A	19860128	US 83554717	A	19831123	198607	
EP 110301	B	19891108				198945	
DE 3380834	G	19891214				198951	

Priority Applications (No Type Date): JP 82207698 A 19821129
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 110301	A	E	30		
Designated States (Regional): DE FR GB NL					
EP 110301	B	E			
Designated States (Regional): DE FR GB NL					

... has scanning electron microscope with dimension measuring section and is for metal crystal, sub- grain **boundary, powder particle** size

...Abstract (Basic): The scanning electron microscope (**SEM**) seams a beam onto a sample, e.g. a **semiconductor wafer** to obtain an image signal corresponding to the sample. An enlarged image of the sample...

...setter which displays cursors on the CRT and a memory which receives signals divided into **picture elements** and stores them as image data. A CPU section receives the stored image data corresponding...

20/3,K/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

04623430 **Image available**
PICTURE PROCESSING METHOD

PUB. NO.: 06-295330 [JP 6295330 A]
PUBLISHED: October 21, 1994 (19941021)
INVENTOR(s): RYUZAKI KOJI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-081822 [JP 9381822]
FILED: April 08, 1993 (19930408)
JOURNAL: Section: , Section No. FFFFFF, Vol. 94, No. 10, Pg. FFFFFF, FF, FFFF (FFFFFFFF)

...JAPIO KEYWORD:Super High Density **Integrated Circuits** , LSI & GS

ABSTRACT
... accuracy of pattern existence, a defect, etc., by processing picture data with uneven gradation, correcting **SEM** picture data including the objective pattern and removing the unevenness of gradation...

... processing by using a filter matrix at least over N times the range of one **picture element** in the 1st picture data and obtaining the 2nd picture data (C) and the 3rd...

20/3,K/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

04315909 **Image available**
METHOD FOR EXTRACTING PATTERN FEATURE

PUB. NO.: 05-307609 [JP 5307609 A]
PUBLISHED: November 19, 1993 (19931119)
INVENTOR(s): KOMATSU BUNRO
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-086362 [JP 9186362]
FILED: March 26, 1991 (19910326)
JOURNAL: Section: P, Section No. 1700, Vol. 18, No. 121, Pg. 107, February 25, 1994 (19940225)

...JAPIO KEYWORD:Super High Density **Integrated Circuits** , LSI & GS

ABSTRACT
...CONSTITUTION: An electron microscope (**SEM**) image is inputted, its observed image is inputted to a frame memory and stored as an original image and then (normal) logarithmical conversion processing is applied to respective **picture elements** (PEs) in the original image. Then N-digit-advance conversion processing is applied to respective...
... memory are searched by an image processor to detect the positions of a pattern. The **pel** addresses of the detected positions are counted up in the X and Y directions, the size value of each **pel** is considered for the sum of the addresses to find out the diameter or peripheral...

... the area of the hole is found out while considering the size value of

each **pel** .

20/3,K/3 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

03627867 **Image available**
DENSITY TRANSFORMING METHOD FOR **SEM** PICTURE AND **SEM** PICTURE TRANSFORMER

PUB. NO.: 03-290767 [JP 3290767 A]
PUBLISHED: December 20, 1991 (19911220)
INVENTOR(s): WATANABE TOSHIBUMI
ITO MINORU
APPLICANT(s): NIPPON TELEGR & TELEPH CORP <NTT> [000422] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-092266 [JP 9092266]
FILED: April 09, 1990 (19900409)
JOURNAL: Section: P, Section No. 1330, Vol. 16, No. 123, Pg. 149, March 27, 1992 (19920327)

DENSITY TRANSFORMING METHOD FOR **SEM** PICTURE AND **SEM** PICTURE TRANSFORMER

ABSTRACT
... obtain pictures, which can be easily observed, corresponding to the specific ity of an electric **circuit** board by setting the upper limit value of a luminance value to be transformed and...
... using the reference substrate of a material and a work process equal to the electric **circuit** board of an observation object...

...CONSTITUTION: A reference substrate 100 and a picture 200 of a scanner type electronic microscope (**SEM**) are prepared with the materials and work processes equal to an electric **circuit** board 101 to be observed, and distribution is calculated for the luminance value of the **SEM** picture 200. From this luminance value distribution, the upper limit luminance value is set. When the luminace value exceeds the upper limit luminance value for each **picture element** of a **SEM** picture 201 of the electric **circuit** board 201, the luminance value is made equal to the upper limit luminance value. When...

... by the luminance value transform function. Thus, density observation transformation is enabled for observing the **SEM** picture 201 of the electric **circuit** board 101.

20/3,K/4 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014421284 **Image available**
WPI Acc No: 2002-241987/200229
XRAM Acc No: C02-072880
XRPX Acc No: N02-186830
Detecting binding of members of a binding pair, by interacting solid support on which first member of binding pair is immobilized and arrayed, with second member, determining spatial distribution of second member
Patent Assignee: EL MUL TECHNOLOGIES LTD (ELMU-N); YEDA RES & DEV CO LTD (YEDA); ZIK O (ZIKO-I)
Inventor: LEVIT-BINNUN N; LINDNER A; MOSES E; ZIK O
Number of Countries: 097 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200214830	A2	20020221	WO 2001IL764	A	20010816	200229	B
AU 200180075	A	20020225	AU 200180075	A	20010816	200245	
EP 1315957	A2	20030604	EP 2001958357	A	20010816	200337	
			WO 2001IL764	A	20010816		

Priority Applications (No Type Date): US 2000225747 P 20000817
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200214830	A2	E	87	G01N-000/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

AU 200180075	A		G01N-000/00	Based on patent WO 200214830
EP 1315957	A2	E	G01N-001/00	Based on patent WO 200214830

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

Abstract (Basic):
... a sample at almost atmospheric pressure. The method can also be carried out with a **Wafer** Inspection Scanning Electron Microscope (WISEM), thus greatly reducing the cost of instrumentation required to implement...

...The figure shows the longitudinal cross-section of an Scanning Electron Microscope (**SEM**) used as a preparate analysis apparatus...
Extension Abstract:
... at a 20 microm resolution. Intensity was determined by taking the average intensity of the **pixels** in corresponding spots in all slides and reducing the average intensity of the **pixels** immediately surrounding the corresponding spots. The gold-probes slides were visualized with a scanning electron microscope (**SEM**). Images of 48 microm squared (for 40 nm gold colloids) or 12 microm squared sized...

20/3,K/5 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012422719 **Image available**
WPI Acc No: 1999-228827/199919
Related WPI Acc No: 2000-637468
XRPX Acc No: N99-169320
Pattern image processing apparatus using scanning electron microscope (SEM) for VLSI element
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: KOMATSU F; MOTOKI H; TSUBUSAKI K
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5887080	A	19990323	US 95379962	A	19950127	199919	B
JP 7220077	A	19950818	JP 948711	A	19940128	199919	
KR 264338	B1	20000816	KR 951766	A	19950128	200134	
JP 3490490	B2	20040126	JP 948711	A	19940128	200410	

Priority Applications (No Type Date): JP 948711 A 19940128
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5887080	A		11	G06K-009/38	
JP 7220077	A		7	G06T-007/00	
KR 264338	B1			G06T-001/00	
JP 3490490	B2		8	G06T-001/00	Previous Publ. patent JP 7220077

Pattern image processing apparatus using scanning electron microscope (SEM) for VLSI element

Abstract (Basic):
... An A/D converter (11) converts the analog image data supplied from **SEM** (1) into digital data. A spatial filter (12) smoothens the digital image data. A histogram processing unit (13) outputs the summation of **pixels** of smoothed image data corresponding to gray level degree. A threshold value setting unit (14) detects two portions at which the **pixel** number of histogram decreases and sets gray level value of these portions as threshold value...

...pattern within pattern images in which successive hole patterns are repeated on very large scale **integration** **circuit** (VLSI...

...The comparison and detection of the same or similar patterns repeated in the **SEM** image are performed by using the area of the pattern and are not performed on...
... **SEM** (1
...Title Terms: **SEM** ;

20/3,K/6 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011659613 **Image available**
WPI Acc No: 1998-076521/199807
XRPX Acc No: N98-061180
Integrated circuit **layout and dimension mapping method - setting and adjusting magnification, voltage and scan of scanning electron microscope using number of selective algorithms**
Patent Assignee: US SEC OF ARMY (USSA)
Inventor: SARTORE R G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5703361	A	19971230	US 96649826	A	19960430	199807	B

Priority Applications (No Type Date): US 96649826 A 19960430
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5703361	A		5	G01N-023/225	

Integrated circuit **layout and dimension mapping method...**

...Abstract (Basic): The method comprises scanning an area of interest on the **integrated** **circuit** with a beam of electrons within a scanning electron microscope (**SEM**), the beam having its' energy level adjusted to irradiate both the insulation material and the conductive layer, monitoring x-ray radiation synchronously with the scanning, at X-Y **pixel** locations within the area of interest, storing a first map of the x-ray radiation monitored at each X-Y **pixel** location during the scanning, re-scanning the area of interest with a beam of electrons...

...and monitoring the x-ray radiation synchronously with the re-scanning, at the X-Y **pixel** locations and storing a second map of the x-ray radiation monitored at each X-Y **pixel** location during the re-scanning ...

...The method further comprises subtracting the x-ray radiation monitored at each X-Y **pixel** location for the second map from the x-ray radiation monitored at each X-Y **pixel** location for the first map, to derive a third map from the x-ray radiation that relates to only the conductive layer at each X-Y **pixel** location...

...USE - Mapping the lateral dimensions and positions of a conductive layer of an **integrated circuit** .
...

...electron beam is adjusted to produce an enhanced map of the conductive layers on the **integrated circuit chip** .

...Title Terms: **CIRCUIT** ;

20/3,K/7 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010561099 **Image available**
WPI Acc No: 1996-058053/199606
XRPX Acc No: N96-048477
Image features extraction method for SEM - by creating non-linear image enhancement pixels to convert to valued process pixels and partially differentiating in X and Y direction to detect boundary of feature
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: KOMATSU F
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5479535	A	19951226	US 92858219	A	19920326	199606	B
			US 94266096	A	19940627		
KR 9613370	B1	19961004	KR 924575	A	19920320	199927	
JP 3034975	B2	20000417	JP 9186362	A	19910326	200024	

Priority Applications (No Type Date): JP 9186362 A 19910326
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5479535	A		10	G06K-009/48	Cont of application US 92858219
JP 3034975	B2		5	G06T-009/20	Previous Publ. patent JP 5307609
KR 9613370	B1			G06F-015/70	

Image features extraction method for SEM - ...

...by creating non-linear image enhancement pixels to convert to valued process pixels and partially differentiating in X and Y direction to detect boundary of feature

...Abstract (Basic): electron microscope in a frame memory. A logarithmic conversion process is performed for each image **pixel** to create non-linear image enhancement **pixels** . Each non-linear image enhancement **pixels** is assigned to a different group each having a corresponding **pixel** value. The **pixels** are converted into valued

process **pixels** . Each valued process **pixel** in each different group has a corresponding **pixel** value. Threshold values for the valued process are obtained by dividing the whole range of gray levels of the **pixels** by a predetermined value...

...The **pixels** are partially differentiated in X- and Y-directions by the CPU. It makes ''0'' the gray levels of **pixels** within the same area divided by the valued process and makes only the boundary between...
...desired feature of the image is determined by detecting the boundary from the partially differentiated **pixels** .
...

...USE/ADVANTAGE - For e.g. pattern obtained during VLSI **circuit** mfr., makes possible extraction of pattern features from single **SEM** image for subject that may be damaged by **SEM** electron beams or suffer change-up due to frame accumulation
...Title Terms: **SEM** ;

20/3,K/8 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

010264197 **Image available**
WPI Acc No: 1995-165452/199522
XRPX Acc No: N95-129968
Semiconductor **device mfg for display element substrate - applies second pattern formation process which forms wiring electrode linked to** pixel **electrode and drain side of** semiconductor **area NoAbstract**
Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7086611	A	19950331	JP 93255179	A	19930917	199522	B

Priority Applications (No Type Date): JP 93255179 A 19930917
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7086611	A		8	H01L-029/786	

Semiconductor **device mfg for display element substrate...**

...applies second pattern formation process which forms wiring electrode linked to pixel **electrode and drain side of** semiconductor **area NoAbstract**
Title Terms: **SEMICONDUCTOR** ;

20/3,K/9 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

009973374 **Image available**
WPI Acc No: 1994-241087/199429
XRPX Acc No: N94-190053
Dimension measuring method for improved precision of particle beam metrology - setting upper and lower reference levels, performing preliminary scan, determining percentage of time intervals that signal lies outside range and adjusting reference levels and offset level
Patent Assignee: METROLOGIX (METR-N)

Inventor: TORO-LIRA G L; ZMRZLI R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5332898	A	19940726	US 9375515	A	19930614	199429	B

Priority Applications (No Type Date): US 9375515 A 19930614
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5332898	A		10	G01N-023/225	

...Abstract (Basic): In other words, the percentage of ''outliers'' in a profile, that is the number of **pixels** that exceed full scale in a video range, is limited to a predetermined percentage, for...

...USE/ADVANTAGE - Critical dimension measurements of, eg **integrated circuit wafers** using , eg scanning electron microscope. Reduces harmonic distortion introduced during signal acquisition and signal processing...
...Title Terms: **SEM** ;

20/3,K/10 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

009874315 **Image available**
WPI Acc No: 1994-154228/199419
XRPX Acc No: N94-121207
SEM display method e.g. for analysing semiconductor **device electrical contact-point hole - determining distribution of** pixels **for each signal amt., and ratio of amt. and CRT luminance for contrast correction NoAbstract**
Patent Assignee: JEOL CO LTD (NIDS)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 6096711	A	19940408	JP 92244777	A	19920914	199419	B

Priority Applications (No Type Date): JP 92244777 A 19920914
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6096711	A		5	H01J-037/22	

SEM display method e.g. for analysing semiconductor **device electrical contact-point hole...**
...determining distribution of pixels **for each signal amt., and ratio of amt. and CRT luminance for contrast correction NoAbstract**
Title Terms: **SEM** ;

20/3,K/11 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

009651544 **Image available**
WPI Acc No: 1993-345094/199343
XRPX Acc No: N93-266420
Fast scanning electron microscope for real-time observation of dynamically loaded material micro-structural response - uses magnetic

deflection coil with lower inductance from reduced number of turns in saddle coil wires and with increased diameter of wires

Patent Assignee: KACHINA TECHNOLOGIES INC (KACH-N)
Inventor: MACKINNON I D R; ROSS T J; WANG M L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5254857	A	19931019	US 91708505	A	19910531	199343	B
			US 92963038	A	19921019		

Priority Applications (No Type Date): US 91708505 A 19910531; US 92963038 A 19921019
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5254857	A		15	H01J-037/28	Cont of application US 91708505

...Abstract (Basic): The **SEM** includes a high speed continuous scanning electron microscope with a spatial resolution of less than...

...a metallic rod, with a rapid electrical pulse applied to the coil, and the continuous **SEM** and the tension and compression shock wave generator are synchronized, so that a succession of...

...Pref. the continuous **SEM** includes low inductance electron beam magnetic deflection coils with ns rise times and adapted to...

...USE/ADVANTAGE - E.g. **semiconductor** film recrystallisation, solid phase transition high temp. superconductor studies, **IC** inspection and metrology. High magnification, large depth of field with temporal resolution less than 100 mus; allows for scan rate of 381 frames per second and 256multiplied by128 **pixel** density in **SEM** image at data acquisition rate of 25 MHz...

20/3,K/12 (Item 9 from file: 350)

DIALOG(R)File 350:Derwent WPIX

004384328
WPI Acc No: 1985-211206/198535
XRPX Acc No: N85-158706

Data format conversion for output to peripheral - has intelligent peripheral effecting conversion for input to printer or VDU

Patent Assignee: CITIZEN WATCH CO LTD (CITL)
Number of Countries: 003 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3505314	A	19850822	DE 3505314	A	19850215	198535	B
GB 2154348	A	19850904	GB 853755	A	19850214	198536	
GB 2154348	B	19870507				198718	
US 4691364	A	19870901	US 85701220	A	19850213	198737	
DE 3505314	C	19890105				198902	

Priority Applications (No Type Date): JP 8424949 A 19840215
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3505314	A		36		

...Abstract (Equivalent): double size and of 8-bit patterns to 6-bit patterns. The bit pattern conversion **circuit** comprises a decoder (DEM) with address signals, **chip** selects signal, write command and

output enable signal inputs from a processor, a data latching...

...to horizontal conversion and expansiom, a summing module (ORM) containing OR-gates, a select module (**SEM**) producing MSB to LSB conversion and drivers (DR...

...USE/ADVANTAGE - Conversion of input **pixel** data to output data compatible with printer or video display. Provides automatic conversion of bit...

...Abstract (Equivalent): data write signal, data latch means constituting an m-row X m-column matrix memory **circuit** ; (2) first data readout means including m groups of gate sections which constitute row-column conversion means, each group of gate sections having n logical product **circuits** having first and second input terminals, the first input terminals of said n logical product **circuits**, of one section of said m groups of gate sections being connected respectively to n...

...flow of said data latch means, the second input terminals of said n logical product **circuits** being connected in common to form a data readout terminal for a corresponding one group...

...bit to 6 bit conversion means, each group of gate sections having m logical product **circuits** having first and second input terminals, the first input terminals of said m logical product **circuits** of one of said plural groups of gate sections being connected to predetermined memory elements...

...sections of said data latch means, the second input terminals of the m logical product **circuits** of one of said plural groups of gate sections being connected in common to form...

25/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014768775 **Image available**
WPI Acc No: 2002-589479/200263
XRPX Acc No: N02-467729

Grain growth degree **analysis method for** semiconductor wafer , **involves calculating ratio of** pixels **whose standardized values exceed preset value, to that of total** pixels **in target zone of image file of** wafer

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU); CHOI S (CHOI-I); CHON S (CHON-I); JUN C (JUNC-I); KIM K (KIMK-I); KIM S (KIMS-I); LEE S (LEES-I); YANG Y (YANG-I)

Inventor: **CHOI S** ; **CHON S** ; **JUN C** ; **KIM K** ; **KIM S** ; **LEE S** ; **YANG Y** ; **CHOI S B** ; **JUN C S** ; JUN S M; KIM G W; **KIM S M** ; **LEE S G** ; **LEE S H** ; **YANG Y S** ; JEON C S; JEON S M

Number of Countries: 005 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020072133	A1	20020613	US 2001977238	A	20011016	200263 B
JP 2002228607	A	20020814	JP 2001313076	A	20011010	200268
KR 2002030674	A	20020425	KR 200061717	A	20001019	200269
KR 347764	B	20020809	KR 200061717	A	20001019	200311
DE 10151396	A1	20030508	DE 1051396	A	20011018	200331
TW 521363	A	20030221	TW 2001119055	A	20010803	200364

Priority Applications (No Type Date): KR 200061717 A 20001019

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020072133	A1		29	H01L-021/66	
JP 2002228607	A		16	G01N-023/225	
KR 2002030674	A			H01L-021/66	
KR 347764	B			H01L-021/66	Previous Publ. patent KR 2002030674
DE 10151396	A1			H01L-021/66	
TW 521363	A			H01L-021/66	

Grain growth degree **analysis method for** semiconductor wafer , **involves calculating ratio of** pixels **whose standardized values exceed preset value, to that of total** pixels **in target zone of image file of** wafer

Inventor: **CHOI S** ...

... **CHON S** ...

... **JUN C** ...
... **KIM K** ...

... **KIM S** ...

... **LEE S** ...

... **YANG Y** ...

... **CHOI S B** ...

... **JUN C S** ...

... **KIM S M** ...

... **LEE S G** ...

... **LEE S H** ...

... **YANG Y S**

Abstract (Basic):
... is selected from an image file generated by scanning a specific surface portion of a **semiconductor wafer** (30). An image data of the **pixels** in the target zone are standardized and compared with a preset threshold value. The **grain growth degree** is determined by obtaining a ratio of **pixels** whose image values exceed the preset value, to that of the total **pixels** in the zone.
... An INDEPENDENT CLAIM is included for **grain growth degree** analysis apparatus...

...For analyzing **grain growth degree** in **semiconductor wafer** .
...

...Analyzes the distribution degree of unevenness with respect to the surface of the **wafer** . Determines **grain growth** rate accurately and rapidly. Increases productivity by reducing analysis time and by improving quality of...

...The figure shows an exploded schematic view of the **grain growth degree** analysis apparatus...

... **Semiconductor wafer** (30
...Title Terms: **SEMICONDUCTOR** ;

File 9:Business & Industry(R) Jul/1994-2004/Oct 13
(c) 2004 The Gale Group
File 15:ABI/Inform(R) 1971-2004/Oct 14
(c) 2004 ProQuest Info&Learning
File 16:Gale Group PROMT(R) 1990-2004/Oct 14
(c) 2004 The Gale Group
File 20:Dialog Global Reporter 1997-2004/Oct 14
(c) 2004 The Dialog Corp.
File 47:Gale Group Magazine DB(TM) 1959-2004/Oct 14
(c) 2004 The Gale group
File 75:TGG Management Contents(R) 86-2004/Oct W1
(c) 2004 The Gale Group
File 80:TGG Aerospace/Def.Mkts(R) 1986-2004/Oct 14
(c) 2004 The Gale Group
File 88:Gale Group Business A.R.T.S. 1976-2004/Oct 13
(c) 2004 The Gale Group
File 98:General Sci Abs/Full-Text 1984-2004/Aug
(c) 2004 The HW Wilson Co.
File 112:UBM Industry News 1998-2004/Jan 27
(c) 2004 United Business Media
File 141:Readers Guide 1983-2004/Aug
(c) 2004 The HW Wilson Co
File 148:Gale Group Trade & Industry DB 1976-2004/Oct 14
(c)2004 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
(c) 1999 The Gale Group
File 275:Gale Group Computer DB(TM) 1983-2004/Oct 14
(c) 2004 The Gale Group
File 264:DIALOG Defense Newsletters 1989-2004/Oct 14
(c) 2004 The Dialog Corp.
File 484:Periodical Abs Plustext 1986-2004/Oct W2
(c) 2004 ProQuest
File 553:Wilson Bus. Abs. FullText 1982-2004/Aug
(c) 2004 The HW Wilson Co
File 570:Gale Group MARS(R) 1984-2004/Oct 14
(c) 2004 The Gale Group
File 608:KR/T Bus.News. 1992-2004/Oct 14
(c)2004 Knight Ridder/Tribune Bus News
File 620:EIU:Viewswire 2004/Oct 07
(c) 2004 Economist Intelligence Unit
File 613:PR Newswire 1999-2004/Oct 13
(c) 2004 PR Newswire Association Inc
File 621:Gale Group New Prod.Annou.(R) 1985-2004/Oct 14
(c) 2004 The Gale Group
File 623:Business Week 1985-2004/Oct 13
(c) 2004 The McGraw-Hill Companies Inc
File 624:McGraw-Hill Publications 1985-2004/Oct 13
(c) 2004 McGraw-Hill Co. Inc
File 634:San Jose Mercury Jun 1985-2004/Oct 13
(c) 2004 San Jose Mercury News
File 635:Business Dateline(R) 1985-2004/Oct 14
(c) 2004 ProQuest Info&Learning
File 636:Gale Group Newsletter DB(TM) 1987-2004/Oct 14
(c) 2004 The Gale Group
File 647:CMP Computer Fulltext 1988-2004/Oct W1
(c) 2004 CMP Media, LLC
File 696:DIALOG Telecom. Newsletters 1995-2004/Oct 13
(c) 2004 The Dialog Corp.
File 674:Computer News Fulltext 1989-2004/Sep W1
(c) 2004 IDG Communications
File 810:Business Wire 1986-1999/Feb 28

File 813:PR Newswire 1987-1999/Apr 30

Set	Items	Description
S1	4242625	SEMICONDUCTOR?? OR WAFER?? OR CIRCUIT?? OR IC OR INTEGRAT?-??(2N)CIRCUIT?? OR CHIP?? OR SEMI()CONDUCT????
S2	43721	(SIZE?? OR DEGREE?? OR AMOUNT?? OR VOLUME?? OR DIMENSION?? OR HEIGHT?? OR GROW??? OR WIDT?? OR INTENSITY?? OR DENSIT??)(-5N)(HSG OR HSGS OR (HEMISPHERICAL??()GRAIN??) OR GRAIN??)
S3	173667	PIXEL?? OR PEL OR (PICTURE??()ELEMENT??) OR SUB()PIX?? OR -SUBPIXEL??
S4	2376	(THRESHOLD?? OR PREDETERMIN??? OR LIMIT??)(5N)S3
S5	8750160	IMAGE?? OR PHOTOGRAPH?? OR PICTURE? ? OR PHOTO??
S6	2147	RATIO??(5N)(PIXEL?? OR PEL OR (PICTURE??()ELEMENT??) OR SU-B()PIX?? OR SUBPIXEL??)
S7	38601	SEM OR SCANNING??(3N)MICROSCOPY??
S8	14877	AU=(JUN C? OR JUN, C? OR CHON S? OR CHON, S? OR CHOI S? OR CHOI, S? OR KIM K? OR KIM, K? OR LEE S? OR LEE, S? OR YANG Y? OR YANG, Y? OR KIM S? OR KIM, S?)
S9	1329	S1(S)S2
S10	72019	S3(S)S5
S11	26	S9 AND S10
S12	15	RD (unique items)
S13	1	S12 AND S7
S14	14	S12 NOT S13
S15	0	S9(S)S4
S16	0	S9(S)S6
S17	878	S8 AND S1
S18	27	S17 AND S7
S19	17	RD (unique items)
S20	0	S19 AND S10
S21	0	S18 AND S10
S22	2	S17 AND S10

13/3,K/1 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

09830772 SUPPLIER NUMBER: 17781359 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Microtexture analysis in aluminum thin films.
Field, David P.; Dingley, David J.
Solid State Technology, v38, n11, p91(5)
Nov, 1995
ISSN: 0038-111X LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 3073 LINE COUNT: 00263

TEXT:
...of the interconnect lines processed from aluminum thin-film structures. Orientation imaging microscopy (OIM), a **SEM** -based imaging technique for analyzing the crystallographic structure of materials, has recently been extended to...
... back-scattering diffraction
and orientation imaging microscopy
EBSD is now a well-established technique in **scanning** electron **microscopy** for obtaining crystallographic data from specimens. When coupled with OIM, it is proving to be...

...form
(MATHEMATICAL EXPRESSION NOT REPRODUCIBLE IN ASCII)
where (x,y) are the coordinates of a **pixel** in the **image** of the EBSD pattern and (Epsilon) takes values from 0 to 180. Each straight line in the **image** transforms to one combined value of ((Rho), (Epsilon)). This can be seen by transposing the...

...Epsilon).
To apply the transform, a two-dimensional accumulator array ((Rho), (Epsilon)) is assigned. The **pixel** intensity at a location (x,y) is measured and that intensity added to the accumulator...

...equation 1 for the given value of (x,y). This process is repeated for all **pixels** (x,y). The summed intensity values in the accumulator are larger for ((Rho), (Epsilon)) values that correspond to a straight line in the **image** that lies along a bright Kikuchi band. The values of ((Rho), (Epsilon)) with the largest...may be important. Considerable microstructure evolution occurs between the thin-film stage and the patterned **wafer** stage of processing. **Grain size** and **grain** boundary structure invariably evolve to lower energy states dependent upon interconnect line geometry.
Conclusion
No...

...23A, pp. 759-767 (1992).
(18.) N.C. Krieger Lassen, D. Juul Jensen, K. Conradsen, **Scanning Microscopy** 6 pp. 115-121 (1992).
(19.) K. Kunze, S.I. Wright, B.L. Adams, D...

14/3,K/1 (Item 1 from file: 15)

02589010 346442691
Analysis of wheel topography and grit force for grinding process modeling
Hecker, Rogelio L; Ramoneda, Igor M; Liang, Steven Y
Journal of Manufacturing Processes v5n1 PP: 13-23 2003
ISSN: 1526-6125 JRNL CODE: JMFP
WORD COUNT: 4079

...ABSTRACT: the grinding wheel topography to evaluate static parameters of the wheel such as the effective **grain** diameter and the static **grain density** as function of the radial distance from the wheel surface. To model the force at each **grain** , the dynamic **grain density** is deduced from the static **grain density** while considering the kinematic effects such as the shadows generated by active grains and the...

... force developed per grain. To calculate these effects, a probabilistic model that estimates the underformed **chip** thickness was used. This model was calibrated and validated based on experimental data of total...
...TEXT: the grinding wheel topography to evaluate static parameters of the wheel such as the effective **grain** diameter and the static **grain density** as function of the radial distance from the wheel surface. To model the force at each **grain** , the dynamic **grain density** is deduced from the static **grain density** while considering the kinematic effects such as the shadows generated by active grains and the...

... force developed per grain. To calculate these effects, a probabilistic model that estimates the undeformed **chip** thickness was used. This model was calibrated and validated based on experimental data of total...

... measured on the wheel at a depth relative to the overall engagement, depends on the **grain size** , wheel porosity, and dressing conditions.

The work of Verkerk and Peters (1977) reviewed different methods...

...to the grain tip geometry.

This paper presents a 3-D methodology to measure the **grain** geometry and the static **grain density** as a function of the wheel penetration. This static **grain density** is then modified to account for kinematic and dynamic effects to calculate the dynamic **grain density** . A model for force per **grain** considering **chip** thickness as a stochastic variable is formulated to incorporate the dynamic effects of grain local... and sufficiently reflective to be useful for the optical interferometry.

The resolution of a microscope **image** is 2.2 x 2.2 microns per **pixel** . Each digitized **image** is processed to extract the wheel surface information in the context of average cutting edge...

...all four individual cross sections.

Figure 1

Wheel Surface Replication

Figure 2

Binary 2-D **Image** from Wheel Surface (180 x 180 **pixels**)

The data are subsequently used to calculate the grain diameter and the static grain density...hardness, the cutting edge effective diameter, and the undeformed chip thickness.
Model Prediction

The dynamic **grain density** , Eq. (6), is a function of the undeformed **chip** thickness, h. However, the dynamic **grain density** itself is a governing factor for **chip** thickness; therefore, its determination is of a closed-loop nature. It was suggested in Hecker and Liang (2003) that this process can be modeled using **chip** thickness as a probabilistic random variable, which was expected to assume a Rayleigh probability density...

... HRC, and the tool was an aluminum oxide specified as 5SG465IVS. The determination of dynamic **grain** density and the force per **grain** requires knowledge of the tool condition and material properties, including the spring constant equivalent for...be concluded that the grain deflection and kinematic shadow play secondary effects on the dynamic **grain density** . On the other hand, the depth of engagement, z, calculated using the **chip** thickness value is the main factor.

Figure 6

Normal and Tangential Forces

The normal and...
... can be a consequence of the dressing conditions imposed on the wheel surface.

The dynamic **grain density** was calculated from the static **grain density** and dynamic effects such as the kinematic shadow generated by active grains and the grain local deflection. The main variable that determines the dynamic **grain density** was the depth of engagement measured radially into the wheel, which is governed by the undeformed **chip** thickness.

The prediction of the normal and the tangential force per grain is presented based...

14/3,K/2 (Item 2 from file: 15)

01807702 04-58693
Big jobs are going to micro-machines
Brown, Stuart F
Fortune v139n9 PP: 128B-128H May 10, 1999
ISSN: 0015-8259 JRNL CODE: FOR
WORD COUNT: 4071

...TEXT: each silicon wafer.

(Photograph Omitted)

Captioned as: Safety lock The small photos show gears the **size** of a pollen **grain** (left) that spin in the prototype "stronglink" (center) developed by Sandia Laboratories for a nuclear bomb. The dozens of components, "grown" fully assembled, all fit on a tiny **chip** .

Analog, a publicly held company whose sales hit $1.2 billion in 1998, has shipped... as stadium spectators who display color cards on command to create images.

The mirrors form **pictures** by flipping into or out of each color's light path at the correct instant...

...per second. By popping up to supply the correct color the mirrors behave like reflecting **pixels** to form a much brighter and crisper **image** , with truer colors, than is possible with conventional equipment. Brightness gradations within a frame are achieved by varying the on-time of the individual mirrors. The **image** the DLP creates is projected through a second lens onto a viewing screen.

Who could...

14/3,K/3 (Item 3 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

00709160 93-58381
Eye tech
Callahan, Sean
Forbes ASAP Supplement PP: 57-67 Jun 7, 1993
ISSN: 0015-6914 JRNL CODE: FBR
WORD COUNT: 3701

...TEXT: NASA) was Eli Arazi, founder of Scitex, the Bedford, Mass., maker of workstations dedicated to **image** processing. Originally started in Israel in 1968 as Scientific Technology, the company first used electronic ...

...separation negatives for printing presses that included software for the manipulation of the most minute **picture elements** (**pixels**). Thus, the age of electronic retouching was born.

By 1988, with increased CPU speeds and...technological barrier, however, is the manufacture of a CCD array that can match, on a **pixel** -to- **pixel** basis, the information in a **photographic** negative of comparable **size** . Today's fine- **grained** 35mm films can capture the equivalent of approximately 18 million **pixels** of usable **photographic** data. The state-of-the-art Kodak DCS 200 digital camera (a modified Nikon 8008 SLR with a Kodak CCD **chip**) registers just 1.6 million **pixels** .

Further, the yield rate in high-resolution CCD manufacture is low; 10 to 15 percent...

14/3,K/4 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

02883254 Supplier Number: 43888698 (USE FORMAT 7 FOR FULLTEXT)
Eye Tech: With digital imaging, computer manipulation, CD-ROM photo storage and madcap morphists transforming the traditional structures of the photography busi
Forbes, pS57
June 7, 1993
Language: English Record Type: Fulltext

Document Type: Magazine/Journal; General Trade
Word Count: 3709

... NASA) was Eli Arazi, founder of Scitex, the Bedford, Mass., maker of workstations dedicated to **image** processing. Originally started in Israel in 1968 as Scientific Technology, the company first used electronic ...

...separation negatives for printing presses that included software for the manipulation of the most minute **picture elements** (**pixels**). Thus, the age of electronic retouching was born.

By 1988, with increased CPU speeds and...technological barrier, however, is the manufacture of a CCD array that can match, on a **pixel** -to-**pixel** basis, the information in a **photographic** negative of comparable **size** . Today's fine- **grained** 35mm films can capture the equivalent of approximately 18 million **pixels** of usable **photographic** data. The state-of-the-art Kodak DCS 200 digital camera (a modified Nikon 8008 SLR with a Kodak CCD **chip**) registers just 1.6 million **pixels** .

Further, the yield rate in high-resolution CCD manufacture is low; 10 to 15 percent...

14/3,K/5 (Item 1 from file: 20)
DIALOG(R)File 20:Dialog Global Reporter
(c) 2004 The Dialog Corp. All rts. reserv.

30395174 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Q2 2003 Kopin Corporation Earnings Conference Call - Part 1
FAIR DISCLOSURE WIRE
July 04, 2003
JOURNAL CODE: WFDW LANGUAGE: English RECORD TYPE: FULLTEXT
WORD COUNT: 4693

... industry's smallest microdisplays to approximately half their previous size. They are now about the **size** of a **grain** of rice. Responding to the needs of customer electronic OEMs, these displays enable our customer...

... We also introduced a color filter VGA, a .4 inch diagonal 640 x 480 color **pixel** display, which is now the world's smallest lowest power color filter VGA resolution display...

... a new consumer product application and revolutionize artists through these low-power (inaudible) and stunning **image** quality. Along with our three new displays, we are introducing several new electronic viewfinder systems...
... late last fall. With an ATV (ph) greenfield view, the CyberEVF 180K gives a virtual **image** of a 19 inch screen at a distance of 5 feet. To introduce this (technical...in Q3 HBT sales as that customer worked out his remaining inventory of second source **wafers** . We do understand that this is only a third quarter event. Longer term, this (inaudible...

14/3,K/6 (Item 1 from file: 47)
DIALOG(R)File 47:Gale Group Magazine DB(TM)
(c) 2004 The Gale group. All rts. reserv.

04298614 SUPPLIER NUMBER: 17200558 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Scenes from a marriage - of optics and electronics.(Conference on Lasers and Electro-Optics and the Quantum Electronics and Laser Science

conference meeting briefs)
Service, Robert F.
Science, v268, n5218, p1702(2)
June 23, 1995
ISSN: 0036-8075 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 1248 LINE COUNT: 00101

... T-rays to a fine point, which is then scanned over the material to be **imaged** . Another lens collects the rays as they emerge from the other side of the target...

...to stored templates to identify the chemical composition of the material at each point, or **pixel** . As the scan progresses over a couple of minutes, tens of thousands of **pixels** are assembled into an overall **image** .
Because water is such a strong absorber of T-rays, the technique can image water...

...matching holes on a palm-top game board. In this case, the ball bearings are **grain** - **sized** **semiconductor** lasers that resemble tiny pyramids with their tops lopped off; the holes are divots with a matching shape, carved in a silicon **wafer** .
To place these lasers in their slots, the researchers simply mix them with ethanol to...

14/3,K/7 (Item 1 from file: 98)
DIALOG(R)File 98:General Sci Abs/Full-Text

04509383 H.W. WILSON RECORD NUMBER: BGSA01009383 (USE FORMAT 7 FOR FULLTEXT)
Little big screen.
Sherman, Erik
Technology Review (Cambridge, Mass.: 1998) v. 104 no5 (June 2001) p. 64-9
SPECIAL FEATURES: il ISSN: 1099-274X
LANGUAGE: English
COUNTRY OF PUBLICATION: United States
WORD COUNT: 2481

(USE FORMAT 7 FOR FULLTEXT)

TEXT:
... of Sunnyvale, CA, for example, makes a handheld device that, in conjunction with glasses, offers **images** 800 **pixels** across and 600 **pixels** high--the same resolution as a standard 35.5-centimeter desktop monitor. Large companies are...

...with Sony's Glasstron and the Eye-Trek from Olympus both giving the viewer an **image** equivalent to a 132-centimeter screen seen from about two meters away.
Of course, this...ingenious solution does away with screens altogether. Microvision, a Bothell, WA, manufacturer, actually projects an **image** , **pixel** by **pixel** , directly onto the viewer's retina. The approach is similar to cathode-ray projection in...

...head-mounted prototype "Nomad"--scheduled for market release this fall--creates a clear, see-through **image** at arm's length even under the brightest daylight conditions. Eurocontrol, the organization that oversees ...board collapses into a compact unit the size of the PDA.

No Monitor Required
A **semiconductor chip** controls red, green and blue light-emitting diodes, each the **size** of a **grain** of salt. The diodes turn on and off according to the color needed for the...

...the light onto a central micromirror.
The micromirror tilts side to side, shining the final **image** onto the retina one **pixel** at a time.
The technology used in these goggles can also be incorporated into cell...

14/3,K/8 (Item 2 from file: 98)
DIALOG(R)File 98:General Sci Abs/Full-Text

03778310 H.W. WILSON RECORD NUMBER: BGSI98028310 (USE FORMAT 7 FOR FULLTEXT)
Digital cameras.
McCreary, Michael D
Scientific American v. 278 no6 (June 1998) p. 102
SPECIAL FEATURES: il ISSN: 0036-8733
LANGUAGE: English
COUNTRY OF PUBLICATION: United States
WORD COUNT: 425

(USE FORMAT 7 FOR FULLTEXT)

TEXT:
... or from a reconnaissance satellite in space.
A CCD is an array of light-sensitive **picture elements** , or **pixels** , each measuring five to 25 microns across. The camera's lens focuses the scene onto this **pixel** array. Just as the resolution of conventional **photographic** film is related to the **size** of the **grain** , the resolution of a CCD **chip** is measured by the number of **pixels** in the array. A digital still camera intended mainly for nonprofessional use has an array of, typically, 640 by 480 **pixels** ; a top-of-the-line professional camera would have an array of millions of **pixels** .
CCD chips are fabricated in a process that requires hundreds of steps and several weeks...

...Microelectronics Division

Eastman Kodak
Photo/Graphic: PHOTONS that fall into the collection region of a **picture element** , or **pixel** , free electrons from the semiconductor's crystal lattice. Thus, the more light falling on the **pixel** , the more electrons that are liberated. Electrical fields trap and isolate the mobile electrons in one **pixel** from those of other **pixels** until the electrons can be read out as an indication of how much light fell on the **pixel** . A tiny color filter over each **pixel** allows **photons** of only one color to pass through into a **pixel** 's collection region.
Photo /Graphic: **PIXELS** are monochrome, so color filters must be used to record a scene's hues. In...

...digital cameras, a color filter array (above) registers the intensity of one color at each **pixel** . Algorithms then consider the color intensities at nearby **pixels** to estimate, by interpolation, the intensity of the other colors at that **pixel** . This information is then used to generate a full-color **image** (below). ...

14/3,K/9 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

11950929 SUPPLIER NUMBER: 61203161 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Pentacene organic thin-film transistors and ICs.
Klauk, Hagen; Jackson, Thomas N.
Solid State Technology, 43, 3, 63
March, 2000
ISSN: 0038-111X LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 3490 LINE COUNT: 00288

... mobility, a large on/off current ratio is required for TFTs to be useful as **pixel** -addressing devices in active matrix displays and **imagers** . Small TFT subthreshold slope and near-zero threshold voltage are also important to reduce the...

...roughness of 1A, and the deposited pentacene film shows good molecular ordering with large, micron- **sized grains** . For comparison, Fig. 2c shows an AFM image of a pentacene film deposited onto the...

14/3,K/10 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

05888080 SUPPLIER NUMBER: 12307801 (USE FORMAT 7 OR 9 FOR FULL TEXT)
So you want to make slides? Choosing the right film recorder.
Carroll, Seamus
AVC Presentation Development & Delivery, v26, n2, p46(4)
Feb, 1992
ISSN: 1062-2683 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 2693 LINE COUNT: 00209

... CRT (5 to 7 inches diagonal0, the sharper the images. When the CRT's phosphor **grains** are more uniformly small in **size** , the images will also appear sharper. In addition, the longer the CRT tube, the easier...be resolved on a given scan line, the finer the spot and the sharper the **image** . Yes and no. There needs to be a balance between the spot size and the...

...If the spot size is too small, there will be noticeable gaps in the final **image** . If the spot size is too large, **pixels** overlap and **image** sharpness is sacrificed.
For 35mm slides, a 4k (4096 X 2732 image is now the...

14/3,K/11 (Item 1 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)

00675983
France: The French National Center for Research on Telecommunications (CNET) is using laser annealing in development of large-screen TV to solve a key component problem--fabrication of large circuit arrays.
Laser Focus February, 1981 p. 40,42+

Such arrays would combine some control **circuitry** with the **picture**

-generating elements, thereby simplifying electrical connections to the matrix of **picture elements** which comprise the screen. The proposed display would be a sandwich, with the front layer...

... response to electrical control signals. The bottom layer would be a silicon-on-glass thinfilm **circuit** . Research on the use of laser annealing to increase the **grain size** of silicon deposited on glass, and thereby improve the electrical properties of the control **circuit** , was described in several papers from CNET at the Opto 80 conference (Paris) 9/30...

14/3,K/12 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01312460 SUPPLIER NUMBER: 07701818 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Point-and-click image analysis. (image processing development systems) (technical)
Flanagan, Dennis E.
ESD: The Electronic System Design Magazine, v19, n9, p53(4)
Sept, 1989
DOCUMENT TYPE: technical ISSN: 0893-2565 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2366 LINE COUNT: 00197

... useful for repetitive use of effective image enhancement procedures--for example, processing images of metallic **wafers** . In this case, the distribution of **grain size** in photoelectric metal substrates needed to be measured. Average **grain size** reveals important information about the photoelectric properties and the efficiency of the material.
Using Optimas...

...all metal grains within the field of view can be calculated to provide statistics about **grain sizes** for substtrate **wafers** . Unfortunately, the metal surface presented noise, making it difficult to detect edges of the grains...
...nearly impossible to count them by simply setting a threshold.
To overcome this problem, the **image** was treated with a median filter; then, a Roberts edge detection was performed. It was...

...counting. The median filter, a 3 X 3 convolution, diminishes noise by replacing the target **pixel** with the median of neighboring **pixels** . The Roberts filter is a two-pass edge detection that finds the grain boundaries while...

14/3,K/13 (Item 1 from file: 623)
DIALOG(R)File 623:Business Week

0476796 (USE FORMAT 7 FOR FULLTEXT)
THE LIGHT FANTASTIC: OPTOELECTRONICS MAY REVOLUTIONIZE COMPUTERS--AND A LOT MORE
John Carey in Washington, with Neil Gross in Tokyo
Business Week, May 10, 1993, Number 3318, Pg 44
JOURNAL CODE: BW
SECTION HEADING: Cover Story
WORD COUNT: 3,007

...TEXT: and other labs put mirrors on each end of tiny, light-producing

regions in the **semiconductor** . When light bounces back and forth between the mirrors, it's amplified until it's...

...make a pure beam of a single wavelength, or color, of light. This device, the **size** of a **grain** of salt, is a **semiconductor** laser. Today, these are at the core of CD players and many other products.

Semiconductor...radical shift in the way a computer processes information. "The real advantage is that an **image** not a bit is the unit of information," says Purdue University physicist David Nolte. "One **image** can contain 1 billion bits." To match fingerprints, for example, computers now search for similarities between two **pictures** by comparing the thousands of individual **pixels** , or dots, that make up each **image** . An optical processor, by contrast, can overlay two **images** and immediately spot similarities. University of Colorado computer scientist Kristina M. Johnson is using this...

SPECIAL FEATURE:
...data.

AT&T, IBM, Honeywell,
Martin Marietta
ILLUSTRATION by jared schneidman
DATA: OPTOELECTRONIC TECHNOLOGY CONSORTIUM

Photograph : A force to be reckoned with David Miller's team at bell labs has built superfast experimental hybrids called smart **pixels** --chips with arrays of both lasers and transistors

DAVID A. ZICKL

Photograph: Seeing the light...

14/3,K/14 (Item 1 from file: 624)
DIALOG(R)File 624:McGraw-Hill Publications

0476796
THE LIGHT FANTASTIC: OPTOELECTRONICS MAY REVOLUTIONIZE COMPUTERS--AND A LOT MORE
Business Week May 10, 1993; Pg 44; Number 3318
Journal Code: BW ISSN: 0007-7135
Section Heading: Cover Story
Word Count: 3,007 *Full text available in Formats 5, 7 and 9*

BYLINE:
John Carey in Washington, with Neil Gross in Tokyo

TEXT:
... and other labs put mirrors on each end of tiny, light-producing regions in the **semiconductor** . When light bounces back and forth between the mirrors, it's amplified until it's...

... make a pure beam of a single wavelength, or color, of light. This device, the **size** of a **grain** of salt, is a **semiconductor** laser. Today, these are at the core of CD players and many other products.

Semiconductor... radical shift in the way a computer processes information. "The real advantage is that an **image** not a bit is the unit

of information," says Purdue University physicist David Nolte. "One **image** can contain 1 billion bits." To match fingerprints, for example, computers now search for similarities between two **pictures** by comparing the thousands of individual **pixels** , or dots, that make up each **image** . An optical processor, by contrast, can overlay two **images** and immediately spot similarities. University of Colorado computer scientist Kristina M. Johnson is using this...

SPECIAL FEATURE:
...data.

AT&T, IBM, Honeywell,
Martin Marietta
ILLUSTRATION by jared schneidman
DATA: OPTOELECTRONIC TECHNOLOGY CONSORTIUM

Photograph : A force to be reckoned with David Miller's team at bell labs has built superfast experimental hybrids called smart **pixels** --chips with arrays of both lasers and transistors

DAVID A. ZICKL

Photograph: Seeing the light...

22/3,K/1 (Item 1 from file: 88)
DIALOG(R)File 88:Gale Group Business A.R.T.S.

05253578 SUPPLIER NUMBER: 57876179
New motion estimation algorithm using adaptively quantized low bit-resolution image and its VLSI architecture for MPEG2 video encoding.(very-large-scale integration; motion pictures expert group)
Lee, Seongsoo ; Kim, Jeong-Min; Chae, Soo-Ik
IEEE Transactions on Circuits and Systems for Video Technology, 8, 6, 734(1)
Oct, 1998
ISSN: 1051-8215 LANGUAGE: English RECORD TYPE: Abstract

Lee, Seongsoo ...

...AUTHOR ABSTRACT: for hardware implementation and substantially reduces the hardware cost by using a low bit-resolution **image** in the block matching. In the low bit-resolution **image** ' generation, adaptive quantization is employed to reduce the bit resolution of the **pixel** values, which is better than simple truncation of the least significant bits in preserving the dynamic range of the **pixel** values. The proposed algorithm consists of two search steps: in the low-resolution search, a...

...MPEG2 motion estimator with a 0.5-((micro)meter) triple-metal CMOS technology. The VLSI **chip** includes 110 K gates of random logic and 90 K bits of SRAM in a...

...size of 11.5 mm x 12.5 mm. The full functionality of the fabricated **chip** was confirmed with an MPEG2 encoder **chip** .
Index Terms - Adaptive quantization block matching, low-resolution search, motion estimation, VLSI.

22/3,K/2 (Item 1 from file: 484)
DIALOG(R)File 484:Periodical Abs Plustext

02653118 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Image enhancement with polymer grid triode arrays
Heeger, Alan J; Heeger, David J; Langan, John; **Yang, Yang**
Science (GSCI), v270 n5242, p1642-1644
Dec 8, 1995
ISSN: 0036-8075 ' JOURNAL CODE: GSCI
DOCUMENT TYPE: Feature
LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 2086 LENGTH: Long (31+ col inches)

... **Yang, Yang**

TEXT:
... Consider the office scene in Fig. 1. (Figure 1 omitted) When the original (14-bit) **image** is displayed with only the dynamic range available on the printed page (about 8 bits...

...are clipped (set to 255), simulating saturation in the region of highest brightness. When the **image** is rescaled (the intensity of each **pixel** was divided by B) and displayed over the same dynamic range (Fig. 1B), it is analogous to the **image** shown on a video display with reduced gain; the features are visible only in the...

...regions. In both cases, a great deal of information contained in the original (14-bit) **image** is lost: in Fig. 1A, the viewer cannot see any detail in the bright regions of the **image** , and in Fig. 1B, the viewer cannot see any detail in the darker regions of the **image** .

Local contrast control involves a combination of logarithmic compression and lateral inhibition, the latter provided...

...directly on an array of photodetectors. Each node of the PGT array corresponds to one **pixel** of the **image** . The array of PGTs with a common grid performs three important functions: (i) The common...

...iii) The PGT array with common grid provides the high input resistance needed for open **circuit** detector operation (4), which results in the logarithmic compression in Eq. 2.

Thus, local contrast...

...is to show that it computes the center-surround difference in Eq. 2. The equivalent **circuit** of ...of sufficient conductivity to make an ohmic contact to the grid, so that the equivalent **circuit** is simplified to a diode in series with a resistor. In the initial experiments, polyvinylcarbazole...

...pixel. Because V sub out oc log I sub L for photovoltaic detectors under open **circuit** conditions, the logarithmic compression of Eq. 1 is straightforward (4).

The PGT-array image processor...

...retina is at an early stage of development. The utility of the PGT array for **image** enhancement will depend on a number of factors--including, for example, sensitivity, noise, dynamic range, and matching from one **pixel** to the next--that must be tested on an engineering prototype.

For a full plastic...

...detector output pad as the anode or cathode of the PGT at that node. The **semiconductor** layers would be cast sequentially from solution and applied onto the detector array much like...

...and on the demultiplexer input.

Alternatively, the PGT array could be used to process the **image** after analog-to-digital conversion and integrated directly into a display (such as a liquid...

...fabricated directly on, as an integral part of, the display: for example, between the control **circuits** and the liquid-crystal layer. The data would be logarithmically compressed digitally and input into the PGT array to process the **image** ; the output from the **pixels** of the array of PGTs would serve as the input to the **pixels** of the display.

REFERENCES AND NOTES

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2. C. Koch and H. Li, Ed., Vision **Chips** : Implementing Vision Algorithms with Analog VLS) **Circuits** (IEEE Computer Society Press, Los Alamitos, CA, 1994).

3. Y. Yang and A. J. Heeger...

...S. patent application 08227,979: Nature 372, 244 (1994).

4. S. M. Size, Physics of **Semiconductor** Devices (Wiley, New York, 1981).

5. M. Reghu et al., Phys. Rev. B 50, 13931...

```
File   2:INSPEC 1969-2004/Oct W1
         (c) 2004 Institution of Electrical Engineers
File   6:NTIS 1964-2004/Oct W1
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2004/Oct W1
         (c) 2004 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2004/Oct W2
         (c) 2004 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2004/Sep
         (c) 2004 ProQuest Info&Learning
File  65:Inside Conferences 1993-2004/Oct W2
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File  94:JICST-EPlus 1985-2004/Sep W2
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File  95:TEME-Technology & Management 1989-2004/Jun W1
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File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Sep
         (c) 2004 The HW Wilson Co.
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         (c) 2004 INIST/CNRS
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File 239:Mathsci 1940-2004/Nov
         (c) 2004 American Mathematical Society
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
File 603:Newspaper Abstracts 1984-1988
         (c)2001 ProQuest Info&Learning
File 483:Newspaper Abs Daily 1986-2004/Oct 13
         (c) 2004 ProQuest Info&Learning
File 248:PIRA 1975-2004/Oct W1
         (c) 2004 Pira International

Set     Items   Description
S1    3494325   SEMICONDUCTOR?? OR WAFER?? OR CIRCUIT?? OR IC OR INTEGRAT?-
            ??(2N)CIRCUIT?? OR CHIP?? OR SEMI()CONDUCT????
S2     288824   (SIZE?? OR DEGREE?? OR AMOUNT?? OR VOLUME?? OR DIMENSION??
            OR HEIGHT?? OR GROW??? OR WIDT?? OR INTENSITY?? OR DENSIT??)(-
            5N)(HSG OR HSGS OR (HEMISPHERICAL??()GRAIN??) OR GRAIN??)
S3     138487   PIXEL?? OR PEL OR (PICTURE??()ELEMENT??) OR SUB()PIX?? OR -
            SUBPIXEL??
S4       2367   (THRESHOLD?? OR PREDETERMIN??? OR LIMIT??)(5N)S3
S5    3618100   IMAGE?? OR PHOTOGRAPH?? OR PICTURE? ? OR PHOTO??
S6       1649   RATIO??(5N)(PIXEL?? OR PEL OR (PICTURE??()ELEMENT??) OR SU-
            B()PIX?? OR SUBPIXEL??)
S7     580480   SEM OR SCANNING??(3N)MICROSCOPY??
S8     235955   AU=(JUN C? OR JUN, C? OR CHON S? OR CHON, S? OR CHOI S? OR
            CHOI, S? OR KIM K? OR KIM, K? OR LEE S? OR LEE, S? OR YANG Y?
            OR YANG, Y? OR KIM S? OR KIM, S?)
S9           1   AU='LEE SANG BONG'
S10    235955   S8 OR S9
S11     20590   S1 AND S2
S12      1092   S11 AND S5
S13         0   S12 AND S4
S14        20   S12 AND S3
S15        12   RD (unique items)
S16       285   S12 AND S7
S17         0   S16 AND S6
S18       251   S10 AND S11
```

S19 0 S18 AND (S3 AND S5)

15/3,K/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6986303 INSPEC Abstract Number: B2001-09-6135E-015, C2001-09-5260B-027
Title: Design issues for hardware implementation of an algorithm for segmenting hyperspectral imagery
Author(s): Theiler, J.; Leeser, M.E.; Estlick, M.; Szymanski, J.J.
Author Affiliation: Space & Remote Sensing Sci. Group, Los Alamos Nat. Lab., NM, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.4132 p.99-106
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 2000 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(2000)4132L.99:DIHI;1-F
Material Identity Number: C574-2001-037
U.S. Copyright Clearance Center Code: 0277-786X/2000/$15.00
Conference Title: Imaging Spectrometry VI
Conference Sponsor: SPIE
Conference Date: 31 July-2 Aug. 2000 Conference Location: San Diego, CA, USA
Language: English
Subfile: B C

Title: Design issues for hardware implementation of an algorithm for segmenting hyperspectral imagery
Abstract: Modern hyperspectral **imagers** can produce data cubes with hundreds of spectral channels and millions of **pixels** . One way to cope with this massive volume is to organize the data so that **pixels** with similar spectral content are clustered together in the same category. This provides both a compression of the data and a segmentation of the **image** that can be useful for other **image** processing tasks downstream. The classic approach for segmentation of multidimensional data is the k-means ...

... a simple algorithm, but the computational expense can be considerable, particularly for clustering large hyperspectral **images** into many categories. The ASAPP (Accelerating Segmentation And **Pixel** Purity) project aims to relieve this processing bottleneck by putting the k-means algorithm into...

... a linear combination of the two), we can fit more distance-computation nodes on the **chip** , obtain a higher **degree** of fine- **grain** parallelism, and therefore faster performance, but at the price of slightly less optimal clusters. We...

... both a theoretical (using random simulated data) and an empirical viewpoint (using 224-channel AVIRIS **images** and 10-channel multispectral **images**).
...Descriptors: **image** classification...

... **image** coding...

... **image** segmentation
Identifiers: hyperspectral **imagers** ; ...

... **image** segmentation...

...multispectral **images** ;

15/3,K/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6917840 INSPEC Abstract Number: A2001-11-4240K-005, B2001-06-4350-026
Title: High resolution digital holography
Author(s): Jacquot, M.; Sandoz, P.; Tribillon, G.
Author Affiliation: Lab. d'Opt. P.M. Duffieux, Univ. de Franche-Comte, Besancon, France
Journal: Optics Communications vol.190, no.1-6 p.87-94
Publisher: Elsevier,
Publication Date: 1 April 2001 Country of Publication: Netherlands
CODEN: OPCOB8 ISSN: 0030-4018
SICI: 0030-4018(20010401)190:1/6L.87:HRDH;1-C
Material Identity Number: O015-2001-009
U.S. Copyright Clearance Center Code: 0030-4018/2001/$20.00
Language: English
Subfile: A B

...Abstract: coupled device cameras require the incident beams to be quasi-parallel. That implies large speckle **grain size** and low lateral resolution in reconstructed **images** . Better lateral resolutions are demonstrated in our work, down to 8 mu m, allowing the...
... The experimental set-up built samples the incident light distribution with a definition of 500 **pixels** mm/sup -1/ The maximum acceptable angle is then widened and the hologram recording and...

... results in phase-contrasts imaging are also reported. The design of dedicated complementary metal-oxide- **semiconductor** active **pixel** sensor cameras is also discussed.
...Descriptors: CCD **image** sensors...

...CMOS **image** sensors...

... **grain size** ; ...

... **image** reconstruction...

... **image** resolution...

...optical **images** ;
...Identifiers: speckle **grain size** ; ...

...reconstructed **images** ; ...
...complementary metal-oxide- **semiconductor** active **pixel** sensor cameras

15/3,K/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6150421 INSPEC Abstract Number: B1999-03-7260D-003
Title: Analysis of image retention in alternating-current thin-film electroluminescent devices
Author(s): Krasnov, A.N.; Hofstra, P.G.; Bajcar, R.C.

Author Affiliation: Luxell Technol. Inc., Mississauga, Ont., Canada
Journal: Journal of Materials Science Letters vol.17, no.19 p. 1673-5
Publisher: Kluwer Academic Publishers,
Publication Date: 1 Oct. 1998 Country of Publication: USA
CODEN: JMSLD5 ISSN: 0261-8028
SICI: 0261-8028(19981001)17:19L.1673:AIRA;1-#
Material Identity Number: H146-1999-002
U.S. Copyright Clearance Center Code: 0261-8028/98/$9.50
Language: English
Subfile: B

Title: Analysis of image **retention in alternating-current thin-film electroluminescent devices**
Abstract: **Image** retention can limit the upper operational frequency of ZnS-based alternating-current thin-film electroluminescent...
... ZnS deposition conditions, the moisture content of the source material, and the drive conditions on **image** retention. Layer-by-layer etching and scanning electron microscopy cross-sectioning techniques were used for...

... this phenomenon. The failure was found to start at the column electrode edges of the **pixel** . Some peculiarities of the **image** -retention phenomenon are discussed, on the basis of an equivalent electrical scheme of the device...

... properties of the active layer. The conditions for producing displays with a reduced occurrence of **image** retention are also discussed.
...Descriptors: II-VI **semiconductors** ; ...

... **image** resolution
...Identifiers: **image** retention...

... **pixel** column electrode edges...

...optimal **grain size** ;

15/3,K/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

5058456 INSPEC Abstract Number: B9511-2570H-002
Title: Considerations for large area fabrication of integrated a-Si and poly-Si TFTs
Author(s): Mei, P.; Anderson, G.B.; Boyce, J.B.; Fork, D.K.; Hack, M.; Johnson, R.I.; Lujan, R.A.; Ready, S.E.
Author Affiliation: Xerox Palo Alto Res. Center, CA, USA
Conference Title: Amorphous Silicon Technology - 1994. Symposium p. 781-6
Editor(s): Schiff, E.A.; Hack, M.; Madam, A.; Powell, M.; Matsuda, A.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1994 Country of Publication: USA xix+903 pp.
Conference Title: Amorphous Silicon Technology - 1994. Symposium
Conference Date: 4-8 April 1994 Conference Location: San Francisco, CA, USA
Language: English
Subfile: B

Abstract: The combination of a-Si low leakage **pixel** TFTs with poly-Si TFTs in peripheral **circuits** provides an excellent method for reducing the number of external connections to large-area imaging...
... displays. To integrate the fabrication of the peripheral poly-Si TFTs with the a-Si **pixel** TFTs, we have developed a three-step laser process which enables selective crystallization of PECVD...

... to those crystallized by a conventional one step laser crystallization of unhydrogenated amorphous silicon. The **grain size** increases with increasing laser energy density up to a peak value of a few microns. The **grain size** decreases with further increases in laser energy density. The transistor field effect mobility is correlated with the **grain size** , increasing gradually with laser energy density until reaching its maximum value. Thereafter, the transistors suffer...
...Descriptors: field effect **integrated circuits** ; ...

... **grain size** ; ...

... **image** sensors...

... **integrated circuit** technology
...Identifiers: low leakage **pixel** TFTs...

...peripheral **circuits** ; ...

... **grain size** ;

15/3,K/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

4986205 INSPEC Abstract Number: B9508-0170L-012, C9508-5260B-103
Title: A single chip **multi-function sensor system for wood inspection**
Author(s): Astrand, E.; Astrom, A.
Author Affiliation: Dept. of Electr. Eng., Linkoping Univ., Sweden
Part vol.3 p.300-4 vol.3
Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA
Publication Date: 1994 Country of Publication: USA 3 vol. (xxvii+875+xxiv+635+xxii+423) pp.
ISBN: 0 8186 6275 1
U.S. Copyright Clearance Center Code: 1051-4651/94/$04.00
Conference Title: Proceedings of 12th International Conference on Pattern Recognition
Conference Sponsor: Int. Association for Pattern Recognition; IEEE Comput. Soc.; Inf. Process. Assoc. Israel
Conference Date: 9-13 Oct. 1994 Conference Location: Jerusalem, Israel
Language: English
Subfile: B C

Title: A single chip **multi-function sensor system for wood inspection**
Abstract: **Image** processing is used in the forest products industry to detect various defects on wood surfaces...

... sensor. Five different measuring principles are simultaneously utilized to detect surface grayscale, surface roughness, deviating **grain** direction, 3D-profile and surface **density** . Using a **pixel** resolution of 1*0.5 mm, the sensor permits scanning of boards at the speed...
...Descriptors: **image** processing...

... **image** processing equipment
Identifiers: single **chip** multifunction sensor system...

... **image** processing...

... **pixel** resolution

15/3,K/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2004 Institution of Electrical Engineers. All rts. reserv.

4772973 INSPEC Abstract Number: A9421-7220J-009, B9411-2520C-008
Title: Investigation of minority carrier diffusion length in multicrystalline silicon by quantitative electron beam induced current mapping
Author(s): Barhdadi, A.; Sivoththaman, S.; Barbe, M.; Rodot, M.; Maurice, J.-L.
Author Affiliation: Lab. de Phys. des Solides de Bellevue, CNRS, Meudon, France
Journal: Diffusion and Defect Data Part B (Solid State Phenomena) vol.37-38 p.189-94
Publication Date: 1994 Country of Publication: Switzerland
CODEN: DDBPE8 ISSN: 1012-0394
Conference Title: Polycrystalline Semiconductors III - Physics and Technology - Third International Conference
Conference Sponsor: Agence Environ. Maitrise de l'Energie; CNRS; et al
Conference Date: 5-10 Sept. 1993 Conference Location: Saint Malo, France
Language: English
Subfile: A B

...Abstract: software has been developed which turns the grey levels of each of the 512*512 **pixels** of a digitised EBIC **image** into diffusion length values. Once the **image** is recorded, the mean value of this parameter in any chosen area of the device...

... The technique is applied for performing quantitative high resolution assessment of diffusion length in large **grain** polycrystalline silicon, in as- **grown** material as well as in fully processed solar cells.
...Descriptors: elemental **semiconductors** ;

15/3,K/7 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
(c) 2004 Elsevier Eng. Info. Inc. All rts. reserv.

04109090 E.I. No: EIP95032620576
Title: Single chip **multi-function sensor for wood inspection**
Author: Astrand, Erik; Astrom, Anders
Corporate Source: Linkoping Univ, Linkoping, Sweden
Conference Title: Proceedings of the 12th IAPR International Conference on Pattern Recognition. Part 3 (of 3)
Conference Location: Jerusalem, Isr Conference Date: 19941009-19941013
E.I. Conference No.: 42601
Source: Proceedings - International Conference on Pattern Recognition v 3 1994. IEEE, Piscataway, NJ, USA,94CH3440-5. p 300-304
Publication Year: 1994
CODEN: PICREG ISSN: 1051-4651

Language: English

Title: Single chip **multi-function sensor for wood inspection**
Abstract: **Image** processing is used in the forest products industry to detect various defects on wood surfaces...

...sensor. Five different measuring principles are simultaneously utilized to detect surface grayscale, surface roughness, deviating **grain** direction, 3D-profile and surface **density** . Using a **pixel** resolution of 1 multiplied by 0.5 mm, the sensor permits scanning of boards at...
Descriptors: **Image** sensors; Imaging systems; **Image** processing; Industrial applications; Inspection; Wood; Defects; Surface properties; Optical resolving power; Scanning
Identifiers: Wood inspection; MAPP2200 **image** processing systems

15/3,K/8 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01844085 ORDER NO: AADAA-I3019718
Techniques and diagnostics on laser recrystallization of thin amorphous silicon films for flat panel display applications
Author: Lee, Ming-Hong
Degree: Ph.D.
Year: 2001
Corporate Source/Institution: University of California, Berkeley (0028)
Source: VOLUME 62/07-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 3352. 104 PAGES
ISBN: 0-493-30942-X

...substrates were suggested. Presently, AMLCDs are mainly manufactured by using a-Si:H for the **pixel** switching device. In order to improve display performance and integrate both the driving **circuitry** and **pixel** TFTs in a monolithic CMOS technology, high quality poly-Si with low defect density and...

...probing of the recrystallization process.
Conventional excimer laser recrystallization (ELC) is studied next. The average **grain size** dependence on laser fluence, number of laser pulses, and film thickness are investigated. Although increasing the number of laser pulses enhances **grain size** , the general problems associated with conventional ELC are narrow process window, nonuniform **grain sizes** , and randomly oriented **grain** boundaries. In order to control the **grain growth** direction, some research efforts have been focused on controlling the temperature distribution in the Si film by using beam shaping techniques. However, the lateral **grain growth** dependence on fluence gradient has not been demonstrated. By shaping the energy profile by using ...

...Nd:YLF laser is irradiated over the molten region. By using high resolution laser flash **photography** , the liquid/solid interface dynamics is observed during the double laser recrystallization process. The lateral ...

...m/s. The revealed resolidification dynamics suggests two crucial factors for inducing ultra-large lateral **grain growth** . First, the formation of nuclei triggered by the nanosecond laser pulse is responsible for seeding the subsequent lateral **grain growth** . Second, the cooling rate into the substrate must be reduced by the Ar<super> +</super> laser so that

sufficient amount of time is allowed for lateral **grain growth** .

15/3,K/9 (Item 2 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01628427 ORDER NO: AAD98-20491
POLYCRYSTALLINE SILICON CONDUCTIVITY MODULATED THIN FILM TRANSISTORS
Author: ANISH, KUMAR K. P.
Degree: PH.D.
Year: 1997
Corporate Source/Institution: HONG KONG UNIV. OF SCI. AND TECH. (PEOPLE'S REPUBLIC OF CHINA) (1223)
Source: VOLUME 59/01-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 338. 133 PAGES

...microelectronic applications. These applications include both niche and large volume applications such as printer drivers, **image** scanners, active-matrix liquid crystal displays (AMLCDs), electro-luminescent displays, plasma assisted displays, etc. Currently...

...it was found that poly-Si material properties vary with its method of preparation, its **grain size** , its surface roughness, and the nature and distribution of the inter-granular and bulk defects...

...invented and fabricated using a simple low temperature poly-Si technology. With these novel structures, **pixels** , **pixel** drivers, and analog and digital peripheral **circuits** can all be built on the same glass substrate. This allows the ultimate goal of...

...high breakdown voltage, and fast switching speed. It is very suitable to be used as **pixel** drivers and high voltage printer drivers.
In order to implement efficient **pixel** transistors and design analog peripheral **circuits** on glass, a second novel structure called the double-gate Elevated-Channel Thin Film Transistor...

...steeper subthreshold slope compared to the uniform film devices. All of these result in efficient **pixels** and high performance analog devices to be built on glass.
Finally, to further optimize the...

15/3,K/10 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04792998 JICST ACCESSION NUMBER: 01A0091400 FILE SEGMENT: JICST-E
Improvement of uniformity in active-matrix light-emitting diodes.
YEH Y-H (1); HAN C-X (1); SHEU C-Y (1); CHUANG F-Y (1); YANG H-L (1); NI F-C (1); WANG W-C (1)
(1) Industrial Technol. Res. Inst., Hsinchu, Twn
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 2000, VOL.100,NO.356(EID2000 90-189), PAGE.97-100, FIG.5, REF.5
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.383:535.35
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

...ABSTRACT: investigated. The non-uniformity feature of LTPS-TFTs is due to the fact that the **grain** boundaries and **sizes** of poly-Si are nearly non-controllable during the laser annealing process. In order to obtain the better uniformity of drive current and performance of gray-scale linearity for AMOLED **pixels** , we suggest that a resistor connected serially to the source terminal of the drive TFT...
...feature dramatically. After measuring the I-V characteristics, a simulation process based on the basic **circuit** theory was proceeded to calculate the characteristics with a serially connected resistor. The calculated results...
...DESCRIPTORS: **pixel** ; ...

... **image** quality
...BROADER DESCRIPTORS: **semiconductor** device...

... **image** ; ...

... **circuit** component...

... **image** characteristic

15/3,K/11 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03546251 JICST ACCESSION NUMBER: 98A0538375 FILE SEGMENT: JICST-E
Smart Arrangement of TFTs in the Peripheral Driver Circuits **for Low-Temperature poly-Si TFT LCD.**
SEGAWA YASUO (1); YAMADA TSUTOMU (1); KIHARA KATSUYA (1); YOKOYAMA RYOICHI (1); YONEDA KIYOSHI (1)
(1) SANYO Electr. Co., Ltd.
Sanyo Tech Rev, 1998, VOL.30,NO.1, PAGE.70-76, FIG.12, TBL.1, REF.6
JOURNAL NUMBER: F0222AAV ISSN NO: 0285-516X CODEN: STRVD
UNIVERSAL DECIMAL CLASSIFICATION: 621.385:621.397
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

Smart Arrangement of TFTs in the Peripheral Driver Circuits **for Low-Temperature poly-Si TFT LCD.**
ABSTRACT: Low-temperature poly-Si TFT LCD has several advantages of capability of **integrating** a driver **circuit** , achieving higher **pixel** density and realizing higher aperture ratio. We propose a smart arrangement of TFTs in the peripheral driver **circuit** to improve the **image** quality of LCD. For this arrangement, TFTs in the horizontal driver **circuit** are aligned oblique to the scanning direction of a sheet beam of excimer laser for...

...TFTs to less than 10%, compared with 35% of the conventional arrangement, so that higher **picture** **image** quality can be achieved. (author abst.)
...DESCRIPTORS: **grain** **size** (crystal...

...driving **circuit** ; ...

... **semiconductor** process

...BROADER DESCRIPTORS: **semiconductor** device...

... **circuit** ;

15/3,K/12 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02623055 JICST ACCESSION NUMBER: 96A0069017 FILE SEGMENT: JICST-E
Development of Optical System Eliminating Insensitive Regions in Linear Image **Sensor Using** Image **Split Mirror.**
MATSUZOE YUJI (1); AKIYAMA NOBUYUKI (2); YACHI TOSHIAKI (3); CHIKAMATSU SHUICHI (3)
(1) Nagaoka Univ. of Technol., Grad. Sch.; (2) Nagaoka Univ. of Technol.; (3) Hitachi Electron. Engineering Co., Ltd.
Seimitsu Kogakkaishi(Journal of the Japan Society for Precision Engineering), 1995, VOL.61,NO.12, PAGE.1715-1719, FIG.13, TBL.1, REF.7
JOURNAL NUMBER: F0268ABQ ISSN NO: 0912-0289
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.08
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

Development of Optical System Eliminating Insensitive Regions in Linear Image **Sensor Using** Image **Split Mirror.**
ABSTRACT: In an automatic detection system for small particles on patterned **wafers**, the optical system which eliminates insensitive regions on a linear **image** sensor has been developed. The real **image** of **wafer** is splitted into two parts by the split mirror set on the real **image** plane of the detection system. The insensitive regions are eliminated by setting the linear **image** sensors whose **pixels** are shifted by a halfpixel relatively, on these two real **images**. The relative displacement between the two real **image** detected by the sensors is 0.5.+-.0.1 **pixel** over the view field of 3mm and the shading of **images** is 23%. The intensity of **images** with the split mirror becomes twice as much as that with the half mirror. (author...
...DESCRIPTORS: **semiconductor** device...

... **wafer** (**IC**); ...

... **image** sensor...

... **grain** **size** analysis...

... **image** formation(optics
...BROADER DESCRIPTORS: solid state **circuit** parts...

... **circuit** component...

... **image** pickup apparatus...

... **photographic** camera

AM RUSH

Access DB# 135034

SEARCH REQUEST FORM

Scientific and Technical Information Center

79178

Requester's Full Name: BRIAN QUANGLE Examiner #: ~~2623~~ Date: 10/13/04

Art Unit: 2623 Phone Number 305-5083 Serial Number: 09/977,238

Mail Box and Bldg/Room Location: PK1 4B40 Results Format Preferred (circle): PAPER DISK E-MAIL

If more than one search is submitted, please prioritize searches in order of need.

****

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: Method and app. for numerically analyzing grain growth on semiconductor wafer using SEM image.

Inventors (please provide full names): HUNG-SAM JUN; SANG-MUN CHON; SANG-BONG CHOI; KYE-WEON, . .

Earliest Priority Filing Date: 10/19/2000

For Sequence Searches Only Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.*

****

STAFF USE ONLY

Searcher: Patel Samir

Searcher Phone #: 306-0254

Searcher Location: PK2-3C03

Date Searcher Picked Up: 2:00PM 10/14

Date Completed: 10:00AM 10/15

Searcher Prep & Review Time: ~~180~~ 210

Clerical Prep Time: _____

Online Time: 60

Type of Search

NA Sequence (#) _____

AA Sequence (#) _____

Structure (#) _____

Bibliographic _____

Litigation _____

Fulltext _____

Patent Family _____

Other _____

Vendors and cost where applicable

STN _____

Dialog ✓

Questel/Orbit _____

Dr.Link _____

Lexis/Nexis _____

Sequence Systems _____

WWW/Internet ✓

Other (specify) _____

PTO-1590 (8-01)

-	2892	HSG or (grow near4 hemispherical near4 grains)	EPO; JPO; DERWENT USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/12 12:47
-	15	(HSG or (grow near4 hemispherical near4 grains)) and ((grow$3 near5 (degree or size or volume or dimension)) same (wafer or semiconductor))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/13 11:43

Search History 10/13/04 6:26:02 PM Page 1

C:\APPS\east\workspaces\09977238.wsp

2/9/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014768775 **Image available**
WPI Acc No: 2002-589479/200263
XRAM Acc No: **N02-467729**

Grain growth degree analysis method for semiconductor wafer, involves calculating ratio of pixels whose standardized values exceed preset value, to that of total pixels in target zone of image file of wafer

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU); CHOI S (CHOI-I); CHON S (CHON-I); JUN C (JUNC-I); KIM K (KIMK-I); KIM S (KIMS-I); LEE S (LEES-I); YANG Y (YANG-I)

Inventor: CHOI S; CHON S; JUN C; KIM K; KIM S; LEE S; YANG Y; CHOI S B; JUN C S; JUN S M; KIM G W; KIM S M; LEE S G; LEE S H; YANG Y S; JEON C S; JEON S M

Number of Countries: 005 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020072133	A1	20020613	US 2001977238	A	20011016	200263 B
JP 2002228607	A	20020814	JP 2001313076	A	20011010	200268
KR 2002030674	A	20020425	KR 200061717	A	20001019	200269
KR 347764	B	20020809	KR 200061717	A	20001019	200311
DE 10151396	A1	20030508	DE 1051396	A	20011018	200331
TW 521363	A	20030221	TW 2001119055	A	20010803	200364

Priority Applications (No Type Date): KR 200061717 A 20001019

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020072133	A1		29	H01L-021/66	
JP 2002228607	A		16	G01N-023/225	
KR 2002030674	A			H01L-021/66	
KR 347764	B			H01L-021/66	Previous Publ. patent KR 2002030674
DE 10151396	A1			H01L-021/66	
TW 521363	A			H01L-021/66	

Abstract (Basic): US 20020072133 A1

NOVELTY - A numerical target zone is selected from an image file generated by scanning a specific surface portion of a semiconductor wafer (30). An image data of the pixels in the target zone are standardized and compared with a preset threshold value. The grain growth degree is determined by obtaining a ratio of pixels whose image values exceed the preset value, to that of the total pixels in the zone.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for grain growth degree analysis apparatus.

USE - For analyzing grain growth degree in semiconductor wafer.

ADVANTAGE - Analyzes the distribution degree of unevenness with respect to the surface of the wafer. Determines grain growth rate accurately and rapidly. Increases productivity by reducing analysis time and by improving quality of devices.

DESCRIPTION OF DRAWING(S) - The figure shows an exploded schematic view of the grain growth degree analysis apparatus.

Semiconductor wafer (30)

pp; 29 DwgNo 1/12

Title Terms: GRAIN; GROWTH; DEGREE; ANALYSE; METHOD; SEMICONDUCTOR; WAFER; CALCULATE; RATIO; PIXEL; STANDARD; VALUE; PRESET; VALUE; TOTAL; PIXEL; TARGET; ZONE; IMAGE; FILE; WAFER

Derwent Class: T01; U11

International Patent Class (Main): G01N-023/225; H01L-021/66

International Patent Class (Additional): G01B-015/00; G01N-023/20;

4/9/1 (Item 1 from file: 350)

012422719 **Image available**
WPI Acc No: 1999-228827/199919
Related WPI Acc No: 2000-637468
XRAM Acc No: **N99-169320**

Pattern image processing apparatus using scanning electron microscope (SEM) for VLSI element

Patent Assignee: TOSHIBA KK (TOKE)
Inventor: KOMATSU F; MOTOKI H; TSUBUSAKI K

Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5887080	A	19990323	US 95379962	A	19950127	199919	B
JP 7220077	A	19950818	JP 948711	A	19940128	199919	
KR 264338	B1	20000816	KR 951766	A	19950128	200134	
JP 3490490	B2	20040126	JP 948711	A	19940128	200410	

Priority Applications (No Type Date): JP 948711 A 19940128
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5887080	A		11	G06K-009/38	
JP 7220077	A		7	G06T-007/00	
KR 264338	B1			G06T-001/00	
JP 3490490	B2		8	G06T-001/00	Previous Publ. patent JP 7220077

Abstract (Basic): US 5887080 A

NOVELTY - A pattern comparison and detection unit (19) sequentially compares each pattern area of a specified pattern with reference image area and detects the pattern having most approximate area. The detected image data corresponding to most approximate area value are output through an output terminal (20).

DETAILED DESCRIPTION - An A/D converter (11) converts the analog image data supplied from SEM (1) into digital data. A spatial filter (12) smoothens the digital image data. A histogram processing unit (13) outputs the summation of pixels of smoothed image data corresponding to gray level degree. A threshold value setting unit (14) detects two portions at which the pixel number of histogram decreases and sets gray level value of these portions as threshold value (slice level). A three value processing unit (15) classified 3 gray level degrees of an intermediate portion, black portion and white pattern.

A noise reduction unit (16) reduces noises from entire image by magnifying black noises on a white background and by reducing white noises on a black background with respect to three valued image data. A pattern area calculating unit (17) specifies a position of patterns for adding a labeling processing to each pattern. A reference image storage unit (18) stores an optimum value as a reference image with respect to an area of each pattern.

USE - For detecting specified hole pattern within pattern images in which successive hole patterns are repeated on very large scale integration circuit (VLSI).

ADVANTAGE - The comparison and detection of the same or similar patterns repeated in the SEM image are performed by using the area of the pattern and are not performed on the shape of the pattern, thereby providing a precise detection result high speed.

DESCRIPTION OF DRAWING(S) - The figure shows block diagram of pattern image processing apparatus.

SEM (1)
A/D converter (11)

5/9/1 (Item 1 from file: 350)

010561099 **Image available**
WPI Acc No: 1996-058053/199606
XRAM Acc No: **N96-048477**

Image features extraction method for SEM - by creating non-linear image enhancement pixels to convert to valued process pixels and partially differentiating in X and Y direction to detect boundary of feature

Patent Assignee: TOSHIBA KK (TOKE)
Inventor: KOMATSU F

Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5479535	A	19951226	US 92858219	A	19920326	199606	B
			US 94266096	A	19940627		
KR 9613370	B1	19961004	KR 924575	A	19920320	199927	
JP 3034975	B2	20000417	JP 9186362	A	19910326	200024	

Priority Applications (No Type Date): JP 9186362 A 19910326
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5479535	A		10	G06K-009/48	Cont of application US 92858219
JP 3034975	B2		5	G06T-009/20	Previous Publ. patent JP 5307609
KR 9613370	B1			G06F-015/70	

Abstract (Basic): US 5479535 A

The method involves storing an image generated by an electron microscope in a frame memory. A logarithmic conversion process is performed for each image pixel to create non-linear image enhancement pixels. Each non-linear image enhancement pixels is assigned to a different group each having a corresponding pixel value. The pixels are converted into valued process pixels. Each valued process pixel in each different group has a corresponding pixel value. Threshold values for the valued process are obtained by dividing the whole range of gray levels of the pixels by a predetermined value.

The pixels are partially differentiated in X- and Y-directions by the CPU. It makes ''0'' the gray levels of pixels within the same area divided by the valued process and makes only the boundary between different areas divided by the valued process have a certain gray level. The desired feature of the image is determined by detecting the boundary from the partially differentiated pixels.

USE/ADVANTAGE - For e.g. pattern obtained during VLSI circuit mfr., makes possible extraction of pattern features from single SEM image for subject that may be damaged by SEM electron beams or suffer change-up due to frame accumulation.

Dwg.1/6

Title Terms: IMAGE; FEATURE; EXTRACT; METHOD; SEM; IMAGE; ENHANCE; PIXEL; CONVERT; VALUE; PROCESS; PIXEL; DIFFERENTIAL; DIRECTION; DETECT; BOUNDARY ; FEATURE
Index Terms/Additional Words: SCANNING; ELECTRON; MICROSCOPE
Derwent Class: T01; T04
International Patent Class (Main): G06F-015/70; G06K-009/48; G06T-009/20
International Patent Class (Additional): G01B-011/24; G06T-005/00
File Segment: EPI
Manual Codes (EPI/S-X): T01-J10B1; T01-J10B2; T04-D07X

3/9/1 **(Item 1 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

004002054
WPI Acc No: 1984-147596/198424
XRAM Acc No: **N84-109740**

Automatic object dimension measuring appts. - has scanning electron microscope with dimension measuring section and is for metal crystal, sub-grain boundary, powder particle size

Patent Assignee: TOKYO SHIBAURA DENKI KK (TOKE)
Inventor: KANO M; NAKAO S; OKUMURA K; YAMAJI H
Number of Countries: 005 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 110301	A	19840613	EP 83111669	A	19831122	198424	B
US 4567364	A	19860128	US 83554717	A	19831123	198607	
EP 110301	B	19891108				198945	
DE 3380834	G	19891214				198951	

Priority Applications (No Type Date): JP 82207698 A 19821129
Cited Patents: 1.Jnl.Ref; A3...8624; DE 2937741; FR 2326030; No-SR.Pub; US 4233510
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 110301	A	E	30		
Designated States (Regional): DE FR GB NL					
EP 110301	B	E			
Designated States (Regional): DE FR GB NL					

Abstract (Basic): EP 110301 A

The scanning electron microscope (SEM) seams a beam onto a sample, e.g. a semiconductor wafer to obtain an image signal corresponding to the sample. An enlarged image of the sample is displayed on a cathode ray tube (CRT).

The dimension measuring section has a setter which displays cursors on the CRT and a memory which receives signals divided into picture elements and stores them as image data. A CPU section receives the stored image data corresponding to a region designated by the cursors, obtains reference points which define two ends of a line corresponding to the dimensions of the sample and calculates the dimensions.

0/14

Abstract (Equivalent): EP 110301 B

A method for measuring the dimensions of an object which is included in a specimen (10), comprising the steps of raster-scanning the specimen (10) with an electron beam (4) so as to obtain an image signal corresponding to the specimen; and measuring the dimensions of the object in accordance with the image signal

obtained in said scanning step; characterized in that said scanning step comprises the steps of aligning the lines of the raster scan substantially parallel to the dimension to be measured; and selecting from said image signal a digital image signal corresponding to a single line of said raster scan; and in that said measuring step includes the steps of

distinguishing in said digital image signal a first portion corresponding to the object, a second portion corresponding to the specimen on one side of the object along the said single scan line and a third portion corresponding to one edge of the object body at the said one side thereof; fitting at least first and third regression lines to said first and third signal portions, respectively, or at

File 348:EUROPEAN PATENTS 1978-2004/Oct W01
(c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20041007,UT=20040930
(c) 2004 WIPO/Univentio

Set	Items	Description
S1	644202	SEMICONDUCTOR?? OR WAFER?? OR CIRCUIT?? OR IC OR INTEGRAT?-??(2N)CIRCUIT?? OR CHIP?? OR SEMI()CONDUCT????
S2	24202	(SIZE?? OR DEGREE?? OR AMOUNT?? OR VOLUME?? OR DIMENSION?? OR HEIGHT?? OR GROW??? OR WIDT?? OR INTENSITY?? OR DENSIT??)(-5N)(HSG OR HSGS OR (HEMISPHERICAL??()GRAIN??) OR GRAIN??)
S3	69870	PIXEL?? OR PEL OR (PICTURE??()ELEMENT??) OR SUB()PIX?? OR -SUBPIXEL??
S4	10544	(THRESHOLD?? OR PREDETERMIN??? OR LIMIT??)(5N)S3
S5	539902	IMAGE?? OR PHOTOGRAPH?? OR PICTURE? ? OR PHOTO??
S6	3319	RATIO??(5N)(PIXEL?? OR PEL OR (PICTURE??()ELEMENT??) OR SUB()PIX?? OR SUBPIXEL??)
S7	28546	SEM OR SCANNING??(3N)MICROSCOPY??
S8	7504	AU=(JUN C? OR JUN, C? OR CHON S? OR CHON, S? OR CHOI S? OR CHOI, S? OR KIM K? OR KIM, K? OR LEE S? OR LEE, S? OR YANG Y? OR YANG, Y? OR KIM S? OR KIM, S?)
S9	1540	S1(S)S2
S10	51672	S5(S)S3
S11	87	S9 AND S10
S12	9	S11 AND S7
S13	0	S12 AND S4 AND S6
S14	42	S11 AND IC=H01L?
S15	35	S14 NOT AD=20001019:20041014/PR
S16	33	S15 NOT S12
S17	1	S16 AND S4
S18	32	S16 NOT S17
S19	2	S18 AND S6
S20	30	S18 NOT S19
S21	2252	S8 AND S1
S22	6	S21(S)S2
S23	0	S22(S)S3

12/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01758353
IC card and booking account system using the IC card
Chipkarte und Buchhaltungssystem unter Verwendung der Chipkarte
Carte a puce et systeme de comptabilite utilisant la carte a puce
PATENT ASSIGNEE:
SEL SEMICONDUCTOR ENERGY LABORATORY CO., LTD., (577861), 398 Hase, Atsugi-shi, Kanagawa-ken 243-0036, (JP), (Applicant designated States: all)
INVENTOR:
Yamazaki, Shunpei, Semiconductor Energy Lab. Co.,Ltd. 398, Hase, Atsugi-shi Kanagawa-ken 243-0036, (JP)
Takayama, Toru, Semiconductor Energy Lab. Co.,Ltd. 398, Hase, Atsugi-shi Kanagawa-ken 243-0036, (JP)
Maruyama, Junya, Semiconductor Energy Lab. Co.,Ltd. 398, Hase, Atsugi-shi Kanagawa-ken 243-0036, (JP)
Goto, Yuugo, Semiconductor Energy Lab. Co.,Ltd. 398, Hase, Atsugi-shi Kanagawa-ken 243-0036, (JP)
Ohno, Yumiko, Semiconductor Energy Lab. Co.,Ltd. 398, Hase, Atsugi-shi Kanagawa-ken 243-0036, (JP)
Akiba, Mai, Semiconductor Energy Lab. Co.,Ltd. 398, Hase, Atsugi-shi Kanagawa-ken 243-0036, (JP)
LEGAL REPRESENTATIVE:
Grunecker, Kinkeldey, Stockmair & Schwanhausser Anwaltssozietat (100721), Maximilianstrasse 58, 80538 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 1437683 A2 040714 (Basic)
APPLICATION (CC, No, Date): EP 2003029021 031216;
PRIORITY (CC, No, Date): JP 2002378853 021227
DESIGNATED STATES: AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES; FI; FR; GB; GR; HU; IE; IT; LI; LU; MC; NL; PT; RO; SE; SI; SK; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK
INTERNATIONAL PATENT CLASS: G06K-019/077
ABSTRACT WORD COUNT: 127
NOTE:
Figure number on first page: 1A

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200429	486
SPEC A	(English)	200429	11825
Total word count - document A			12311
Total word count - document B			0
Total word count - documents A + B			12311

...SPECIFICATION integrated circuit and a display device formed over a plastic substrate.

Fig. 16 is a **SEM** cross-sectional photograph of the sample used in Embodiment 5;

Fig. 17 shows a measured...

...degree)C to 550 (degree)C.

It is possible to obtain crystals having a large **grain size** by emitting a laser beam of second to fourth harmonics of a fundamental harmonic with...

...an elliptical shape on a surface to be irradiated by using an optical system. The **semiconductor** film 505 is irradiated with the

above-described laser beam. On this occasion, an energy...emitting element may be emitted from the side of the card substrate. In this case, **images** displayed in a **pixel** portion is seen in the side of the card substrate.

The light emitting device of...and 1503 denotes a CPU that is one of integrated circuits.

Fig. 15B is a **photograph** of a display device formed over a polycarbonate substrate of 200 (mu)m in thickness. The display device shown in Fig. 15B is a light emitting device, and the **photograph** is taken from the side of the polycarbonate substrate. Reference number 1504 denotes a signal line driver circuit, 1505 denotes a scanning line driver circuit, and 1506 denotes a **pixel** portion. Fig. 15C shows enlarged views of the **pixel** portion 1506 of the light emitting device shown in Fig. 15B. A light emitting element is provided with each **pixels** as shown in Fig. 15C. Light emitted from the light emitting element emits toward the...

...the second substrate.

Fig. 16 is a cross-sectional photograph of a scanning electron microscope (**SEM**) of the sample used in this embodiment. No. 20 denotes the first plastic substrate, No...

12/3,K/2 (Item 2 from file: 348)

01446647

Semiconductor device and manufacturing method thereof
Halbleiterbauelement und dessen Herstellungsverfahren
Dispositif semi-conducteur et son procede de fabrication

PATENT ASSIGNEE:
SEL SEMICONDUCTOR ENERGY LABORATORY CO., LTD., (577861), 398 Hase, Atsugi-shi, Kanagawa-ken 243-0036, (JP), (Applicant designated States: all)
INVENTOR:
Yamazaki, Shunpei, Semiconductor Energy Lab. Co., Ltd., 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036, (JP)
Suzawa, Hideomi, Semiconductor Energy Lab. Co., Ltd., 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036, (JP)
Kusuyama, Yoshihiro, Semiconductor Energy Lab. Co., Ltd., 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036, (JP)
Ono, Koji, Semiconductor Energy Lab. Co., Ltd., 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036, (JP)
Koyama, Jun, Semiconductor Energy Lab. Co., Ltd., 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036, (JP)
LEGAL REPRESENTATIVE:
Grunecker, Kinkeldey, Stockmair & Schwanhausser Anwaltssozietat (100721), Maximilianstrasse 58, 80538 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 1237195 A2 020904 (Basic)
APPLICATION (CC, No, Date): EP 2002004670 020228;
PRIORITY (CC, No, Date): JP 200156063 010228; JP 2001302687 010928
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: H01L-027/12; H01L-021/84
ABSTRACT WORD COUNT: 114
NOTE:
Figure number on first page: 9

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200236	783
SPEC A	(English)	200236	14025
Total word count - document A			14808
Total word count - document B			0
Total word count - documents A + B			14808

...SPECIFICATION display device is particularly demanded.
Conventionally, a liquid crystal display device is known as the **image** display device. Since a high resolution **image** is obtained as compared with a passive liquid crystal display device, an active matrix liquid...

...is used in many cases. According to the active matrix liquid crystal display device, when **pixel** electrodes arranged in matrix are driven, a display pattern is formed on a screen. In more detail, when a voltage is applied between a selected **pixel** electrode and an opposite electrode corresponding to the selected **pixel** electrode, a liquid crystal layer located between the **pixel** electrode and the opposite electrode is optically modulated and the optical modulation is recognized as... devices;
Figs. 12A and 12B show examples of electronic devices;
Fig. 13 is an observation **SEM** picture after etching;
Fig. 14 is an observation **SEM** picture after etching;
Fig. 15 shows a relationship between reliability (20-hours assurance voltage and...oscillation laser may also be used. In order to obtain a crystal with a large **grain size** at crystallization of the amorphous **semiconductor** film, it is preferable that a solid laser capable of producing continuous oscillation is used...

...MW/cm2) (preferably, 0.1 MW/cm2) to 10 MW/cm2)) is required . Then, the **semiconductor** film may be moved relatively to laser light at a speed of about 10 cm...of this embodiment. Fig. 13 is a picture obtained by observing the sample using an **SEM** immediately after etching is performed under the same condition as the above-mentioned first etching ...of this embodiment. Fig. 14 is a picture obtained by observing the sample using an **SEM** immediately after etching is performed under the same condition as the above-mentioned first etching...

12/3,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01076791
Mo-W material for formation of wiring, Mo-W target and method for production thereof, and Mo-W wiring thin film
Molybdan-Wolfram Werkstoff fur Leitungsdrahte, Molybdan-Wolfram Fangelektrode und ihre Herstellungsverfahren, und Molybdan-Wolfram Legierung fur Dunnschichtdrahte
Alliage molybdene-tungstene pour conducteurs electriques, alliage molybdene-tungstene pour cibles et procede pour leur fabrication et alliage molybdene-tungstene pour conducteurs a couche mince
PATENT ASSIGNEE:
KABUSHIKI KAISHA TOSHIBA, (213130), 72, Horikawa-cho, Saiwai-ku, Kawasaki-shi, Kanagawa-ken 210-8572, (JP), (Applicant designated States: all)
INVENTOR:
Kohsaka, Yasuo, 168-1-501, Sengen-cho 3-chome, Nishi-ku, Yokohama-shi,

Kanagawa 220-0072, (JP)
Fukasawa, Yoshiharu, 347-7, Izumi-cho, Izumi-ku, Yokohama-shi, Kanagawa 245, (JP)
Tsuji, Yoshiko, 2-8-14-102, Kokan-dori, Kawasaki-ku, Kawasaki-shi, Kanagawa-ken 210-0852, (JP)
Ikeda, Mitsushi, 2-3-20-711, Taru-machi, Kohoku-ku, Yokohama-shi, Kanagawa 222, (JP)
Sato, Michio, 488-7-1-205, Sugeta-cho, Kanagawa-ku, Yokohama-shi, Kanagawa 221, (JP)
Maki, Toshihiro, 2-63-34, Hino, Konan-ku, Yokohama-shi, Kanagawa-ken 234-0051, (JP)

LEGAL REPRESENTATIVE:
March, Gary Clifford (52654), Batchellor, Kirk & Co. 102-108 Clerkenwell Road, London EC1M 5SA, (GB)

PATENT (CC, No, Kind, Date): EP 947593 A2 991006 (Basic)
EP 947593 A3 991215
APPLICATION (CC, No, Date): EP 99201616 941214;
PRIORITY (CC, No, Date): JP 93312936 931214
DESIGNATED STATES: AT; DE; FR; GB
RELATED PARENT NUMBER(S) - PN (AN):
EP 735152 (EP 95902950)
INTERNATIONAL PATENT CLASS: C22C-027/04; C23C-014/34
ABSTRACT WORD COUNT: 179
NOTE:
Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9940	382
SPEC A	(English)	9940	9488
Total word count - document A			9870
Total word count - document B			0
Total word count - documents A + B			9870

...SPECIFICATION 5b are deposited. Then, through the medium of the gate insulating film 3, an ITO **picture element** electrode 8 is formed. Subsequently, an Al source electrode 6a having a part thereof connected ...

...6b having a part thereof connected to the n+) a-Si layer 5b and the **picture element** electrode 8, and data wirings are simultaneously formed.

The conventional TFT shown in Fig. 4 has a **picture element** electrode and data wirings formed in one and the same layer without intervention by an...

...and data wirings laid out first, an interlayer insulating film subsequently formed thereon, and a **picture element** electrode finally superposed thereon has been conceived and studied as a possible measure of improvement...

...etchant for use on the interlayer insulating film and to the ITO etchant for the **picture element** electrode.

(2) For the purpose of improving the step coverage of the interlayer insulating film thereby heightening the insulation between the data wirings and the **picture element** electrode, the data wirings should be capable of being tapered.

Since none of the wiring...the like. It is, therefore, capable of exalting the insulation between the data wirings and **picture element** electrodes. Owing to these features, liquid crystal display devices of

high reliability can be realized...5b each in 50 nm. Subsequently, ITO was sputtered in 120 nm to form a **picture element** electrode 8. The portion of SiOx)) in the contact part was etched with dilute hydrofluoric ...

...was determined by observing the section of a sample thin film with the aid of **SEM** and measuring the angle of the thin film with the glass substrate. It is clearly...

...varying compositions mentioned above were treated with the etchant for ITO, a material for the **picture element** electrode, BHF, an etchant for the interlayer insulating film, and the etchant for Al to...rate in the rate of about 3 to 10 nm/min, for example) and a **picture element** electrode 18 was formed in a thickness of 120 nm by sputtering ITO.
The Mo...

...which would be used for etching a Mo film or a W film.
In the **picture element** array consequently formed, since the data wirings were given a tapering work, the interlayer insulating...

...could be formed by etching with hydrofluoric acid on the drain electrode 16b and the **picture element** electrode could be worked with a mixed liquid consisting of chlorine with nitric acid. Moreover...

...was formed and a contact hole was formed on the drain electrode 26b, and a **picture element** electrode 28 was formed.
According to Example 3 described above, the effect obtained in Example ...W targets obtained in Example 4 and Referential Example mentioned above were tested for relative **density** , average particle diameter of **grains** , and Vickers hardness. The results were as shown in Table 4 and Table 5. These...

...in place in a DC magnetron sputter device and sputtered on a 6-inch Si **wafer** to form a Mo-W alloy film (in a thickness of 30 nm). The Mo...

...after removal of edge portions 5 mm in width from the relevant 6-inch Si **wafers** . The results of this visual examination are additionally shown in Table 4 and Table 5...

12/3,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01044304
Thin -film semiconductor device, its manufacture and display sytem
Dunnschicht-Halbleiteranordnung, ihre Herstellung und Anzeigsystem
Dispositif semiconducteur a film mince, son procede de fabrication et systeme d'affichage
PATENT ASSIGNEE:
SEIKO EPSON CORPORATION, (730004), 4-1, Nishishinjuku 2-chome, Shinjuku-ku, Tokyo 163-0811, (JP), (Proprietor designated states: all)
INVENTOR:
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Matsueda, Yojiro, c/o Seiko Epson Corporation, 3-5, Owa 3-chome, Suwa-shi, Nagano-ken 392, (JP)
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LEGAL REPRESENTATIVE:

Hoffmann, Eckart, Dipl.-Ing. (5571), Patentanwalt, Bahnhofstrasse 103, 82166 Grafelfing, (DE)
PATENT (CC, No, Kind, Date): EP 923138 A2 990616 (Basic)
EP 923138 A3 990804
EP 923138 B1 021030
APPLICATION (CC, No, Date): EP 99101740 940726;
PRIORITY (CC, No, Date): JP 93184134 930726; JP 94122838 940603
DESIGNATED STATES: DE; FR; GB; IT; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 663697 (EP 94921817)
INTERNATIONAL PATENT CLASS: H01L-029/786; H01L-021/205; G02F-001/136; H01L-021/336
ABSTRACT WORD COUNT: 154
NOTE:
Figure number on first page: 42

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199924	2270
CLAIMS B	(English)	200244	456
CLAIMS B	(German)	200244	410
CLAIMS B	(French)	200244	567
SPEC A	(English)	199924	32610
SPEC B	(English)	200244	29178
Total word count - document A			34886
Total word count - document B			30611
Total word count - documents A + B			65497

...SPECIFICATION or through a level-shifter circuit; whereby an analog signal is supplied to each of **picture elements** in a dot-sequential manner. This enables the construction of an extremely compact data driver ...

...second-stage analog latches are input; whereby an analog signal is supplied to each of **picture elements** in a line-sequential manner. This enables a large active-matrix type of LCD to...

...which outputs of the second-stage latches are input; whereby digital signals are supplied to **picture elements** . This enables the construction of a large-scale digital data driver, which interfaces a digital...among deposition temperature, deposition rate, and carrier mobility;

Fig. 4 is a scanning electron microscope (**SEM**) photograph of the crystal structure of a silicon film (after thermal oxidation, deposition temperature = 510...

...is used in a thin film semiconductor device;

Fig. 5 is a scanning electron microscope (**SEM**) photograph of the crystal structure of a silicon film (after thermal oxidation, deposition temperature = 600...to illustrate the principle of the present invention;

Fig. 9 is a scanning electron microscope (**SEM**) photograph of the amorphous state of a silicon film (before thermal oxidation, deposition temperature = 510...

...be used in a thin film semiconductor device;

Fig. 12 is a scanning electron microscope (**SEM**) photograph of the crystal structure of a silicon film (after thermal oxidation, deposition temperature = 570...

has been believed that regions called...nm(12.9 A)/minute. The presence of islands that can not be verified by **SEM** , as shown in Fig. 9, is verified with AFM, as shown in Fig. 10. Fig...

...amorphous state) deposited at 570(degree)C, and Fig. 12 is a scanning electron microscope (**SEM**) photograph showing the silicon film in a polycrystalline state after thermal oxidation of this film...
...no more than 10,000 nm2). Note that Fig. 13 is a scanning electron microscope (**SEM**) photograph showing a silicon film in a polycrystalline state before thermal oxidation (an as-deposited...

...are distributing in the range of more than 100 nm in diameter, then the average **grain size** of the polycrystalline **semiconductor** film obtained after thermal oxidation will be increased to 10,000 nm2) or more in area, and thus a high-performance thin-film **semiconductor** device will be fabricated.

Although this second example has been described with reference to an... is 370(degree)C.

In Fig. 14, if the deposition temperature is less than 500(**degree**)C, the **grain** area becomes less, but this is when the reactant gas is mono-silane. This does...

...deposition rate high. However, this is not the case for di-silane.

D. Roughness of **Semiconductor** Film and Gate Insulation film Surfaces

In general, when an oxide film is formed by...insulation film is removed by a 10% aqueous solution of hydrogen fluoride to have a SEM observation of the surface of the polycrystalline silicon film after the oxidation, it will show...the thermal oxidation temperature is reduced..

Figs. 19, 20, and 21 are scanning electron microscope (**SEM**) photographs showing the state of a MOS boundary surface of the thin-film semiconductor device...

...and 900(degree)C, respectively. Similarly, Figs. 22, 23, and 24 are scanning electron microscope (**SEM**) photographs showing the state of a MOS boundary surface of the thin-film semiconductor device...the initial a-Si film of this example is made up of large regions, the **size** of the crystal **grains** after the crystallization is also large, thus providing high-performance electrical characteristics. In other words...in the nucleus generation rate between substrates can be made small. In other words, the **size** of **grains** making up the **semiconductor** film, which is of polycrystalline silicon after the thermal oxidation, can be made constant between...

...CLAIMS or through a level-shifter circuit, whereby an analog signal is supplied to each of **picture elements** in a dot-sequential manner.
30. A display system as defined in any oneof claims...

...second-stage analog latches are input; whereby an analog signal is supplied to each of **picture elements** in a line-sequential manner.

31. A display system as defined in any one of...

...which outputs of said second-stage latches are input, whereby digital signals are supplied to **picture elements** .
32. A display system as defined in any one of claims 21 to 24, further...

12/3,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00708300

MOLYBDENUM-TUNGSTEN MATERIAL FOR WIRING, MOLYBDENUM-TUNGSTEN TARGET FOR WIRING, PROCESS FOR PRODUCING THE SAME, AND MOLYBDENUM-TUNGSTEN WIRING THIN FILM

MOLYBDAN-WOLFRAM-MATERIAL ZUM VERDRAHTEN, MOLYBDAN-WOLFRAM-TARGET ZUM VERDRAHTEN, VERFAHREN ZU DEREN HERSTELLUNG UND DUNNE MOLYBDAN-WOLFRAM VERDRAHTUNG

MATERIAU EN MOLYBDENE-TUNGSTENE POUR CABLAGE, CIBLE EN MOLYBDENE-TUNGSTENE POUR CABLAGE, PROCEDE DE FABRICATION ET COUCHE MINCE DE CABLAGE EN MOLYBDENE-TUNGSTENE

PATENT ASSIGNEE:
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TSUJI, Yoshiko, 1-2-2-101, Watarida Kawasaki-ku, Kawasaki-shi Kanagawa 210, (JP)
IKEDA, Mitsushi, 2-3-20-711, Taru-machi Kohoku-ku, Yokohama-shi Kanagawa 222, (JP)
SATO, Michio, 488-7-1-205, Sugeta-cho Kanagawa-ku, Yokohama-shi Kanagawa 221, (JP)
MAKI, Toshihiro, 3-8-15-P2-101, Konan Konan-ku, Yokohama-shi Kanagawa 233, (JP)
LEGAL REPRESENTATIVE:
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PATENT (CC, No, Kind, Date): EP 735152 A1 961002 (Basic)
EP 735152 A1 970226
EP 735152 B1 020417
WO 9516797 950622
APPLICATION (CC, No, Date): EP 95902950 941214; WO 94JP2095 941214
PRIORITY (CC, No, Date): JP 93312936 931214
DESIGNATED STATES: AT; DE; FR; GB
RELATED DIVISIONAL NUMBER(S) - PN (AN):
EP 947593 (EP 99201616)
INTERNATIONAL PATENT CLASS: C22C-027/04; C23C-014/34
ABSTRACT WORD COUNT: 133

LANGUAGE (Publication,Procedural,Application): English; English; Japanese
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	534
CLAIMS B	(English)	200216	721
CLAIMS B	(German)	200216	646
CLAIMS B	(French)	200216	798
SPEC A	(English)	EPAB96	9510
SPEC B	(English)	200216	9544
Total word count - document A			10046
Total word count - document B			11709
Total word count - documents A + B			21755

...SPECIFICATION 5b are deposited. Then, through the medium of the gate insulating film 3, an ITO **picture element** electrode 8 is formed. Subsequently, an Al source electrode 6a having a part thereof connected

...after removal of edge portions 5 mm in width from the relevant 6-inch Si **wafers** . The results of this visual examination are additionally shown in Table 4 and Table 5...

12/3,K/6 (Item 1 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

01036973 **Image available**

HALOGEN-RESISTANT, ANODIZED ALUMINUM FOR USE IN SEMICONDUCTOR PROCESSING APPARATUS

ALUMINIUM ANODISE ET RESISTANT AUX HALOGENES UTILISE DANS UN APPAREIL DE TRAITEMENT DE SEMI-CONDUCTEUR

Patent Applicant/Assignee:
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Legal Representative:
BERNADICOU Michael A (et al) (agent), Blakely, Sokoloff, Taylor & Zafman, LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, CA 90025, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200366920 A1 20030814 (WO 0366920)
Application: WO 2003US3558 20030204 (PCT/WO US0303558)
Priority Application: US 200271869 20020208
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
CN JP KR SG
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT SE SI SK TR
Publication Language: English
Filing Language: English
Fulltext Word Count: 8658

Fulltext Availability:
Detailed Description

Detailed Description
... about 330 'C to relieve stress while reducing the possibility of an increase in the **size** of particulates formed at aluminum **grain** boundaries during the heat treatment, and where an electrochemically applied aluminum oxide protective fihn applied...analysis technique used to determine particle size and size distribution was based on back scattered **image** analysis under the scanning electron microscope (**SEM**). The equipment used to conduct measurements was a KLA TENCORS Surf Scan machine. The magnification was at 500x in order to assess the constituent particles. The area of each **image** was about 150 4m x 200 1,tm. The digital resolution was at least 0.2 4m/ **pixel** . At least 40 **images** were taken at random from a sample area of 0.75 inch diameter in order...

...of various areas on the metal microstructure, to ensure meaningful statistical analysis. The back scattered **images** were digitally stored to provide for statistical analysis. The **images** were transferred to an **image** analyzer and the distribution of the particles with a mean atomic number higher than that of Al (white in the **images**) were detected and measured. The digital resolution allowed for measurement of particles as small as 0.2 /2m. The **image** analyzer used was EBAS by Zeiss. Particle agglomerates were seen as precipitated particles. The parameters...

12/3,K/7 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00950219 **Image available**
MICROLENS FOR PROJECTION LITHOGRAPHY AND METHOD OF PREPARATION THEREOF
MICROLENTILLE POUR GRAVURE PAR PROJECTION ET SON PROCEDE DE PREPARATION
Patent Applicant/Assignee:
PRESIDENT AND FELLOWS OF HARVARD COLLEGE, Holyoke Center, Suite 727, 1350 Massachusetts Avenue, Cambridge, MA 02138, US, US (Residence), US (Nationality)
Inventor(s):
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WHITESIDES George M, 124 Grasmere Street, Newton, MA 02158, US,
PAUL Kateri E, 910 Rich Ave, Apt 5, Mountain View, CA 94040, US,
Legal Representative:
POMIANEK Michael J (agent), Wolf, Greenfield & Sacks, P.C., 600 Atlantic Avenue, Boston, MA 02210, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200284340 A1 20021024 (WO 0284340)
Application: WO 2002US11623 20020410 (PCT/WO US0211623)
Priority Application: US 2001283102 20010410
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 24709

Fulltext Availability:
Detailed Description
Claims

Detailed Description
... along with the corresponding object pattern masks utilized to fabricate the patterns
(positioned below each **SEM** micrograph copy);
FIG. 4A-4D are photocopies of micrographs of microlens arrays comprising various microoptical...the surface (e.g., microinanipulation, etc.) could be employed.

FIGS. 3A-3C are photocopies of **SEM** micrographs of ...array and, in

Claim
... for use as a photonic crystal.

88 The method as in claim 64, wherein the **image** surface comprises an **image** pattern including a plurality of discrete features, wherein the features are suitable for use as a **pixel** array.

89 The method as in claim 64, wherein the image surface comprises an image...

12/3,K/8 (Item 3 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00933012 **Image available**
WIDE BAND GAP SEMICONDUCTOR COMPOSITE DETECTOR PLATES FOR X-RAY DIGITAL RADIOGRAPHY
PLAQUES DE DETECTEUR COMPOSITES DE SEMI-CONDUCTEUR A ECART A LARGE BANDE POUR RADIOGRAPHIE NUMERIQUE A RAYONS X
Patent Applicant/Assignee:
REAL-TIME RADIOGRAPHY LTD, Building 1B, Jerusalem Technology Park, 91487 Jerusalem, IL, IL (Residence), IL (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
HAREL Ze'ev, Hakomemiut Street 2/13, 43414 Ra'anana, IL, IL (Residence), IL (Nationality), (Designated only for: US)
SCHIEBER Michael, Bartenura Street 9, 92105 Jerusalem, IL, IL (Residence), IL (Nationality), (Designated only for: US)
SAADO Yehezkel, Rav Tzair Street 5, 96146 Jerusalem, IL, IL (Residence), IL (Nationality), (Designated only for: US)
HERMON Haim, Bar Kochva Street 4/2, 97875 Jerusalem, IL, IL (Residence), IL (Nationality), (Designated only for: US)
MEERSON Evgeny, Yosi Ben Yo'ezer Street 12, 93301 Jerusalem, IL, IL (Residence), IL (Nationality), (Designated only for: US)
REISMAN Benjamin Joshua, Halamish, 71945 M.P. Modi'in, IL, IL (Residence), IL (Nationality), (Designated only for: US)
Legal Representative:
JEREMY M BEN-DAVID & CO LTD (agent), Har Hotzvim Hi-Tech Park, P.O. Box 45087, 91450 Jerusalem, IL,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200267014 A1 20020829 (WO 0267014)
Application: WO 2002IL124 20020218 (PCT/WO IL0200124)
Priority Application: IL 141483 20010218; IL 143849 20010619
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 12705
Fulltext Availability:
Detailed Description
Claims

least two said **semiconductors** selected from bismuth iodide, lead iodide, mercuric iodide, thallium bromide and cadmium-zinc-telluride (CZT ...

...least two discrete composition layers, each of said discrete layers comprised of at least one **semiconductor** selected from a group consisting of bismuth iodide, lead iodide, mercuric iodide, thallium bromide and...

...at least two discrete composition layers comprise at least one discrete composition layer where said **semiconductor** is non-heat treated, non-ground particulate lead iodide and at least one discrete composition layer where said **semiconductor** is non-heat treated, nonground particulate mercuric iodide.

38 An image receptor according to claim...

12/3,K/9 (Item 4 from file: 349)

00405083 **Image available**

CRYSTALLIZATION PROCESSING OF SEMICONDUCTOR FILM REGIONS ON A SUBSTRATE, AND DEVICES MADE THEREWITH

PROCEDE DE CRISTALLISATION DE REGIONS D'UNE COUCHE DE SEMI-CONDUCTEUR SUR UN SUBSTRAT, ET DISPOSITIFS REALISES SELON CE PROCEDE

Patent Applicant/Assignee:
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IM James S,
SONG Hyun Jin,
SPOSILI Robert S,
YOON Jung H,
Inventor(s):
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SONG Hyun Jin,
SPOSILI Robert S,
YOON Jung H,

Patent and Priority Information (Country, Number, Date):
Patent: WO 9745827 A1 19971204
Application: WO 96US7730 19960528 (PCT/WO US9607730)
Priority Application: WO 96US7730 19960528
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
CA JP US
Publication Language: English
Fulltext Word Count: 5441

Fulltext Availability:
Detailed Description

English Abstract
...laterally from a seed area of the film. The semiconductor devices can be included as **pixel** controllers and drivers in liquid-crystal display devices, and in **image** sensors, static random-access memories (SRAM), silicon-on-insulator (SOI) devices, and three-dimensional integrated...

French Abstract
...Les dispositifs a semi-conducteur peuvent etre introduits en tant que

dispositifs de commande de **pixels** et dispositifs d'attaque, dans des dispositifs d'affichage a cristaux liquides, et dans des detecteurs d' **images** , des memoires RAM statiques, des dispositifs du type silicium sur isolant, et des dispositifs a...

Detailed Description
... quartz or glass substrate, for example,
This technology is in use in the manufacture of **image** sensors and active-matrix liquid-crystal display (AMLCD) devices. In the latter, in a regular...

...of thin-film
transistors (TFT) on an appropriate transparent substrate, each transistor serves as a **pixel** controller.

In commercially available AMLCD devices, the thin-film transistors are formed in hydrogenated amorphous...

...technique can be used in
the manufacture of high-speed liquid crystal display devices, wherein **pixel** controllers or/and driver circuitry are made in single-crystal or regular/quasi regular polycrystalline films, other applications include **image** sensors, static random-access memories (SRAM), silicon-on-insulator (SOI) devices, and threedimensional integrated circuit...subsequent to irradiation, the films were thoroughly defect-etched using Secco etchant and examined using **scanning** electron **microscopy** (**SEM**), The largest, most uniform grains were obtained at a back
2
side energy density of...may have to be reduced in length, and the semiconductor surface may become irregular where **grains** **growing** from opposite directions come together during the solidification process, An oxide cap may be formed...window portion 121 is
transparent. The display window portion 121 includes a regular array of **pixels** 122, each including a TFT **pixel** controller, Each **pixel** controller can be individually addressed by drivers 123, Preferably, **pixel** controllers or/and driver circuitry are implemented in semiconductor material processed in accordance with the technique of the present invention,
other applications include **image** sensors,
static random-access memories (SRAM), silicon-on insulator (SOI) devices, and three-dimensional integrated...

17/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00543489
Liquid crystal display device
Flussigkristall-Anzeigevorrichtung
Dispositif d'affichage a cristal liquide
PATENT ASSIGNEE:
SONY CORPORATION, (214024), 6-7-35 Kitashinagawa Shinagawa-ku, Tokyo, (JP), (applicant designated states: DE;FR;GB)
INVENTOR:
Ino, Masumitsu, c/o Patents Division, Sony Corporation, 6-7-35 Kitashinagawa, Tokyo 141, (JP)
LEGAL REPRESENTATIVE:
Robinson, Nigel Alexander Julian et al (69551), D. Young & Co., 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 531124 A1 930310 (Basic)
EP 531124 B1 961127
APPLICATION (CC, No, Date): EP 92307986 920903;
PRIORITY (CC, No, Date): JP 91224352 910904; JP 91354801 911219; JP 91354805 911219
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G02F-001/136; **H01L-027/12**
ABSTRACT WORD COUNT: 210

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPAB96	769
CLAIMS B	(German)	EPAB96	681
CLAIMS B	(French)	EPAB96	816
SPEC B	(English)	EPAB96	10610
Total word count - document A			0
Total word count - document B			12876
Total word count - documents A + B			12876

...INTERNATIONAL PATENT CLASS: **H01L-027/12**

...SPECIFICATION there is disclosed an active matrix substrate having a large capacitor in a liquid crystal **picture element** section without reducing aperture ratio. Figure 39 shows a structure of such a capacitor for...

...storing capacitor 202 as a capacitor element, and a liquid crystal cell 203 constituting a **picture element** . The active matrix type liquid crystal display device having such a structure is driven in...
...1)) to S(sub(n)). Immediately thereafter, the display signal is written to the corresponding **picture element** . The display signal written into the **picture element** is held for one field period by the liquid crystal cell 203 and the capacitor...

...next field. Thus, alternating current drive of the liquid crystal is effected.

The larger the **picture element** capacitance of each liquid crystal cell 203, the more securely a **picture element** potential can be held, so that non-uniformity of contrast can be suppressed to thereby secure a fixed display quality. Accordingly, in the case that the **picture element** electrode area is large (for example, 200(sup(2)(mu)m(sup(2) or more), it is unnecessary to provide the capacitor element 202.

film transistor (103) formed in one of said plurality of first trenches and associated with said **picture element** electrode and a capacitor element (104) associated with said **picture element** electrode.

7. A liquid crystal display device according to claim 6, wherein said plurality of...

19/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01071891
METHOD OF PRODUCING SILICON OXIDE FILM, METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE, DISPLAY, AND INFRARED IRRADIATING DEVICE
VERFAHREN ZUR HERSTELLUNG EINES SILIZIUMOXIDFILMS, VERFAHREN ZUR HERSTELLUNG EINER HALBLEITERVORRICHTUNG, HALBLEITERVORRICHTUNG, ANZEIGE UND INFRAROT BESTRAHLUNGSANLAGE
PROCEDE POUR PRODUIRE UN FILM D'OXYDE DE SILICIUM, PROCEDE POUR FABRIQUER UN DISPOSITIF A SEMI-CONDUCTEURS, DISPOSITIF A SEMI-CONDUCTEURS, AFFICHAGE ET DISPOSITIF DE RAYONNEMENT INFRAROUGE
PATENT ASSIGNEE:
SEIKO EPSON CORPORATION, (730004), 4-1, Nishishinjuku 2-chome, Shinjuku-ku, Tokyo 163-0811, (JP), (Applicant designated States: all)
MITSUBISHI DENKI KABUSHIKI KAISHA, (208589), 2-3, Marunouchi 2-chome Chiyoda-ku, Tokyo 100-8310, (JP), (Applicant designated States: all)
INVENTOR:
MIYASAKA, Mitsutoshi, Seiko Epson Corp., 3-5, Owa 3-chome, Suwa-shi, Nagano-ken 392-8502, (JP)
SAKAMOTO, Takao, Mitsubishi Denki K. K., 2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-8310 100-8310, (JP)
LEGAL REPRESENTATIVE:
Hoffmann, Eckart, Dipl.-Ing. (5571), Patentanwalt, Bahnhofstrasse 103, 82166 Grafelfing, (DE)
PATENT (CC, No, Kind, Date): EP 966029 A1 991222 (Basic)
WO 9934431 990708
APPLICATION (CC, No, Date): EP 98961631 981225; WO 98JP5991 981225
PRIORITY (CC, No, Date): JP 97361567 971226
DESIGNATED STATES: DE; GB; NL
INTERNATIONAL PATENT CLASS: **H01L-021/316** ; C23C-016/40; **H01L-029/786** ; **H01L-021/336**
ABSTRACT WORD COUNT: 97
NOTE:
Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; Japanese
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199951	1382
SPEC A	(English)	199951	10863
Total word count - document A			12245
Total word count - document B			0
Total word count - documents A + B			12245

INTERNATIONAL PATENT CLASS: **H01L-021/316** ...

... **H01L-029/786** ...

... **H01L-021/336**

...SPECIFICATION quartz glass substrate can also be regarded as the first silicon oxide film.

Next, a **semiconductor** film is formed on a dielectric material where at least a surface in contact with the **semiconductor** film is the first silicon oxide film. In this step of forming a **semiconductor** film, a high energy body such as a laser beam or heat is supplied to this **semiconductor** film after film deposition by a vapor deposition method or the like, thus processing the melt crystallization or the solid phase

crystallization of the **semiconductor** film. If the initially deposited thin film is amorphous or a mixed crystal structure which...

...chlorine (XeCl) excimer laser. Due to the irradiation thereof, at least the surface of a **semiconductor** thin film is molten and crystallized. There is an excellent characteristic in that crystal grains...

...difficult: if the irradiation energy density of the excimer laser or the like onto the **semiconductor** thin film is slightly larger than an appropriate level, it is realized that the **size** of crystal **grains** of the polycrystalline film is suddenly reduced by the amount between 1/10 and 1/100 and, in the worst case, the **semiconductor** film will disappear. Therefore, in the present invention, the melt-crystallization of a **semiconductor** film is carried out by setting an irradiation laser energy density lower than an appropriate...

...to about 50mJ(center dot)cm-2). As a result the melt-crystallization of a **semiconductor** film will be carried out with stability. Of course, the crystalline quality of the polycrystalline **semiconductor** film is not very high under this condition; however, there is a step of irradiating ...NMOS thin film semiconductor device obtained in the Second Embodiment as a switching element for **picture elements** of a color LCD having 200 (row) x 320 (column) x 3 (color) = 192,000 (**picture elements**), an active matrix substrate was manufactured wherein a 6-bit digital data driver (column side...

...The output from the CMOS analog switch is connected to the source line of the **picture element** section. The capacitance of the D/A converter section satisfy the relations: C0)) = C1))/2 = C2))/4 = C3))/8 = C4))/16 = C5))/32. Digital **image** signals output from the video random access memory (VRAM) of a computer can be directly input to the digital **image** signal line. The **picture elements** of the active matrix substrate of the Third Embodiment include source electrodes and source wirings, and the drain electrodes (**picture element** electrodes) include aluminum, forming a reflective LCD.

A liquid crystal panel is manufactured wherein the...the scanning driver operate normally at a wide operation area; and moreover, since the aperture **ratio** is high regarding the **picture element** section, a liquid crystal display device of high display quality is fabricated even with the...

19/3,K/2 (Item 2 from file: 348)

00730471

Display device and manufacture method for the same
Anzeigevorrichtung und Verfahren zu ihrer Herstellung
Dispositif d'affichage et son procede de fabrication

PATENT ASSIGNEE:
CANON KABUSHIKI KAISHA, (542361), 30-2, 3-chome, Shimomaruko, Ohta-ku, Tokyo, (JP), (Proprietor designated states: all)
INVENTOR:
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Miyawaki, Mamoru, c/o Canon K.K., 30-2, 3-chome Shimomaruko, Ohta-ku, Tokyo, (JP)
Inoue, Shunsuke, c/o Canon K.K., 30-2, 3-chome Shimomaruko, Ohta-ku, Tokyo, (JP)

Kochi, Tetsunobu, c/o Canon K.K., 30-2, 3-chome Shimomaruko, Ohta-ku, Tokyo, (JP)
LEGAL REPRESENTATIVE:
Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. 2-5 Warwick Court, High Holborn, London WC1R 5DH, (GB)
PATENT (CC, No, Kind, Date): EP 689085 A2 951227 (Basic)
EP 689085 A3 970108
EP 689085 B1 030129
APPLICATION (CC, No, Date): EP 95304240 950619;
PRIORITY (CC, No, Date): JP 94137319 940620; JP 94137320 940620; JP 94137321 940620
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: G02F-001/136; **H01L-027/12**
ABSTRACT WORD COUNT: 83
NOTE:
Figure number on first page: 3

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	788
CLAIMS B	(English)	200305	412
CLAIMS B	(German)	200305	342
CLAIMS B	(French)	200305	482
SPEC A	(English)	EPAB96	11555
SPEC B	(English)	200305	10239
Total word count - document A			12345
Total word count - document B			11475
Total word count - documents A + B			23820

...INTERNATIONAL PATENT CLASS: **H01L-027/12**

...SPECIFICATION devices using liquid crystals, there has recently been a demand for producing a finer display **image** . Particularly, the so-called active matrix type display panel using thin film switching devices to drive **pixels** is relatively easy to increase the number of **pixels** and the number of gradation steps as compared with other types of liquid crystal display...

...current in the sub-threshold region is not satisfactory. Also, due to variations in the **grain size** of p-Si and changes in the process conditions, the carrier mobility and the rising...satisfactory characteristics. The use of unsatisfactory p-SiTFTs has raised characteristic limitations in making up **circuits** such as a shift register for driving pixels.

SUMMARY OF THE INVENTION

A primary object of the present invention is to provide a display device which can display a finer **image** with the increased number of **pixels** by using p-SiTFTs that have sufficiently high carrier mobility and a good on/off...

...is to provide a transmission type liquid crystal display device which can display a finer **image** with the increased number of **pixels** . Still another object of the present invention is to provide a projection or spectacle type...

...display device which can utilize light at a high rate and can display a finer **image** with the increased number of **pixels** .

To solve the technical problems explained above and to achieve the foregoing objects, the display...

A sixth embodiment will be described...
...substrate) where the Si substrate 1 has been partly etched away to form a transparent **pixel** display area. 5 denotes a portion at which the field oxide film 3 terminates. 6...

...Embodiment 5. The resulting display panel was superior and able to display a high-quality **image** stably for a long period of time.

(Embodiment 7)
A seventh embodiment will be described...

...to Fig. 28. Fig. 28 schematically shows arrangements of a thin film transistor (TFT), a **pixel** electrode, wirings and so on which are formed the semiconductor substrate shown in Fig. 26...

...channel portion of the TFT, 902 is an interlayer insulating layer, and 903 is a **pixel** electrode (ITO). 904 is a low-concentration source/drain layer close to a gate, 906...

...Embodiment 5. The resulting display panel was superior and able to display a high-quality **image** stably for a long period of time. The technique described in this embodiment can be...
...reference to Fig. 29. Fig. 29 schematically shows part of a semiconductor substrate with a **pixel** electrode, wirings and so on omitted. In Fig. 29, components denoted by the same reference...
Embodiment 5. The resulting display panel was superior and able to display a high-quality **image** stably for a long period of time. Consequently, this embodiment can provide a display device which has the good mechanical strength and can stably display a high-quality **image** .

20/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01619342
Fabrication method for a thin film semiconductor device, the thin film semiconductor device itself, liquid crystal display, and electronic device
Herstellungsmethode fur eine Anordnung mit einem dunnen Halbleiterfilm, die Anordnung selber und Flussigkristallanzeige
Methode de fabrication d'un dispositif semiconducteur a couche mince, dispositif semiconducteur et dispositif d'affichage a cristal liquide
PATENT ASSIGNEE:
SEIKO EPSON CORPORATION, (730004), 4-1, Nishishinjuku 2-chome, Shinjuku-ku, Tokyo 163-0811, (JP), (Applicant designated States: all)
INVENTOR:
Miyasaka, Mitsutoshi, Seiko Epson Cor., 3-5, Owa 3-chome, Suwa-shi, Nagano-ken 392-8502, (JP)
LEGAL REPRESENTATIVE:
Hoffmann, Eckart, Dipl.-Ing. (5571), Patentanwalt, Bahnhofstrasse 103, 82166 Grafelfing, (DE)
PATENT (CC, No, Kind, Date): EP 1335419 A2 030813 (Basic)
EP 1335419 A3 030827
APPLICATION (CC, No, Date): EP 2003008849 950615;
PRIORITY (CC, No, Date): JP 94133374 940615; JP 9572144 950329
DESIGNATED STATES: DE; FR; GB
RELATED PARENT NUMBER(S) - PN (AN):
EP 714140 (EP 95921972)
INTERNATIONAL PATENT CLASS: **H01L-021/205** ; **H01L-029/49** ; **H01L-021/336** ; **H01L-029/786** ; G02F-001/136
ABSTRACT WORD COUNT: 114
NOTE:
Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200333	216
SPEC A	(English)	200333	22853
Total word count - document A			23069
Total word count - document B			0
Total word count - documents A + B			23069

INTERNATIONAL PATENT CLASS: **H01L-021/205** ...

... **H01L-029/49** ...
... **H01L-021/336** ...

... **H01L-029/786**

...SPECIFICATION temperatures between room temperature and approximately 400(degree)C.

In the present invention, because the **semiconductor** layer formed on top of the underlevel protection layer functions as the active layer for the transistor and this **semiconductor** layer is formed by crystallization, the properties of the underlevel protection layer have a strong influence on the quality of the **semiconductor** layer. First, it is desirable to have the center line mean surface roughness of the underlevel protection layer be 3.0 nm or less. When a **semiconductor** film such as silicon is deposited by CVD on top of an underlevel

protection layer...

...is low, the regions constituting the film will become large. If the regions in the **semiconductor** film prior to crystallization are large, the grains constituting the crystallized film will also be large. When the grains in the **semiconductor** film are large, the electrical properties, such as mobility, of the **semiconductor** device having an active layer comprised of these grains improve. According to the experiments of...

...3.0 nm or less with the result being the ability to fabricate high performance **semiconductor** devices. The reason for this seems to be that the irregularity in the surface of...

...surface roughness of the underlevel protection layer be 1.5 nm or less when the **semiconductor** layer is melt crystallized. If the surface is this smooth, the melted **semiconductor** material such as silicon spreads readily over the underlevel protection layer. Because of this, large diameter **grains** can **grow** easily; and the properties of the thin film **semiconductor** device ...At the same time, local agglomeration of the molten material during solidification of the melted **semiconductor** material does not occur; and the uniformity within the molten region increases. The LSI scaling law applies to thin film **semiconductor** devices as well; and it appears that the miniaturization of elements will continue in step...

...submicron order, how to avoid local agglomeration will be an important issue. When fabricating the **semiconductor** layer by melt crystallization, the center line mean surface roughness of the underlevel protection layer...

...By meeting this criterion, it is possible to produce uniform films, without local agglomeration, from **semiconductor** films with large-diameter grains.

Another role of the underlevel protection layer is to prevent...will almost disappear. From about 150 nm (1500 A) to 200 nm (2000 A), the **size** of the crystal **grains** will gradually increase along with the film thickness. At 200 nm (2000 A) or higher, the film will **grow** while the crystal **grains** maintain approximately the same shape. The film thickness dependency of the transistor properties will also...

...Put another way, in the case of this invention, transistor properties are the best at **semiconductor** film thicknesses from 20 nm (200 A) to 150 nm (1500 A), but ideally between...

...with the thickness of the film. The principles of off state leakage in thin film **semiconductor** device are not well understood. In this invention, the principles are unclear; but, if the...

...ideally from 40 nm (400 A) to 100 nm (1000 A). When the thin film **semiconductor** device of this invention is used in an LCD, it is desirable to consider the...

...Light exposure will cause an increase in the off state leakage current in thin film **semiconductor** devices. This is called the optical leakage current. Having a sufficiently small optical leakage current is a condition for a good thin film **semiconductor** device. In the case of the thin film **semiconductor** device of this ...off state leakage and optical leakage are important, such as when using a thin film **semiconductor** device for the pixel switching element of an LCD, it is desirable to have a **semiconductor** film thickness from 10 nm (100 A) to 70 nm (700 A). Moreover, when it...

...carry out activation in a stable manner, a lower limit must be set for the **semiconductor** film thickness. With this invention, the desired value is 30 nm (300 A) or higher...

...thickness of 50 nm (500 A) or higher is desired.

2-10. Crystallization of the **Semiconductor** Film through VHS-PECVD and Microwave PECVD

As described in detail in section (2-8...At the same time, because the a-Si layer is composed of large regions, the **size** of the **grains** after crystallization is large and high-performance electrical characteristics can be obtained. In other words...matrix liquid crystal display device (LCD), high-definition LCDs (LCDs having a large number of **picture elements**), bright LCDs (LCDs having a high aperture ratio in which storage capacitors have been reduced or eliminated), and highly-integrated LCDs (LCDs having a large number of **picture elements** per unit area), all of which were heretofore impossible using a-Si TFTs of the...

20/3,K/2 (Item 2 from file: 348)

01208990

METHOD AND APPARATUS FOR LASER HEAT TREATMENT, AND SEMICONDUCTOR DEVICE

VERFAHREN UND APPARAT ZUR WARMEBEHANDLUNG DURCH LASERSTRAHLEN, UND HALBLEITERANORDNUNG

PROCEDE ET APPAREIL DE TRAITEMENT THERMIQUE PAR LASER, ET DISPOSITIF SEMI-CONDUCTEUR

PATENT ASSIGNEE:
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PATENT (CC, No, Kind, Date): EP 1087429 A1 010328 (Basic)
WO 0054314 000914
APPLICATION (CC, No, Date): EP 907924 000308; WO 00JP1375 000308
PRIORITY (CC, No, Date): JP 9963107 990310; JP 9990439 990331
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: **H01L-021/268** ; **H01L-021/20**
ABSTRACT WORD COUNT: 66
NOTE:

Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; Japanese
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200113	774
SPEC A	(English)	200113	8786
Total word count - document A			9560
Total word count - document B			0
Total word count - documents A + B			9560

INTERNATIONAL PATENT CLASS: **H01L-021/268** ...

... **H01L-021/20**

...SPECIFICATION transistor, and a semiconductor device produced using such method and apparatus.

Background Art

At present, **pixel** portions of a liquid crystal panel produce an **image** by switching of thin film transistors that are formed from an amorphous or polycrystalline silicon...

...substrate. If a driver circuit (which is now typically independently mounted outside) for driving the **pixel** transistors can be simultaneously formed on the panel, significant advantages would be obtained in terms...dielectric compound, or a high-temperature superconductor has the same effect of achieving a large **grain size** even if it is subjected to the above-mentioned laser heat treatment.

Embodiment 2

In...

...eliminated, whereby the carriers are not scattered at the boundary planes. Moreover, the crystal-defect **density** at the **grain** boundaries is reduced due to the extremely small grain boundaries, whereby the mobility of the...

...high frequency can be obtained. Moreover, in the method of present invention, not only the **grain size** and thus the mobility of the transistor are increased, but also the conditions for obtaining...at the irradiation intensity of approximately 100 mJ/cm2) or more. In view of the **grain size** , mobility of the transistor upon making a **semiconductor**0 device, and the like, 400 mJ/cm2) or more is preferred.

Embodiment 5

In Embodiment...Under such conditions, the laser heat treatment of the amorphous silicon film was conducted. The **grain size** of the resultant polycrystalline silicon film was as follows: when the maximum gradient of the...

...different due to the difference in length of the grains. In order to make an **integrated circuit** requiring high speed and functionality, the mobility of approximately 100 cm2)/Vs is required. Accordingly...

...compound, or a high-temperature superconductor compound has the same effect of achieving a large **grain size** even if it is subjected to the above-mentioned laser heat treatment.

In Embodiment 10...

20/3,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01038361
Thin film transistor with a LDD structure and method of producing the same
Dunnfilmtransistor mit einer LDD Struktur und Verfahren zur Herstellung
Transistor a couche mince avec une structure LDD et sa methode de fabrication
PATENT ASSIGNEE:
MATSUSHITA ELECTRONICS CORPORATION, (456134), 1-1, Saiwai-cho, Takatsuki-shi, Osaka 569, (JP), (Applicant designated States: all)
INVENTOR:
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Ito, Yutaka, 2035 City-Inn Liberte, 2-9-7, Shinkanaya, Uozu-shi, Toyama, 937-0801, (JP)
LEGAL REPRESENTATIVE:
Kugele, Bernhard et al (51541), NOVAPAT INTERNATIONAL SA, 9, Rue du Valais, 1202 Geneve, (CH)
PATENT (CC, No, Kind, Date): EP 921576 A2 990609 (Basic)
EP 921576 A3 991103
APPLICATION (CC, No, Date): EP 98122700 981130;
PRIORITY (CC, No, Date): JP 97333883 971204
DESIGNATED STATES: DE; FR; GB; NL
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: **H01L-029/786** ; **H01L-021/336**
ABSTRACT WORD COUNT: 105
NOTE:
Figure number on first page: 1A 1B

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9923	265
SPEC A	(English)	9923	2389
Total word count - document A			2654
Total word count - document B			0
Total word count - documents A + B			2654

INTERNATIONAL PATENT CLASS: **H01L-029/786** ...

... **H01L-021/336**

...ABSTRACT A2
On the polycrystal **semiconductor** film 3 formed on the insulating substrate 1, the source 6 and drain 7 in...
...measured from the edge of gate insulating film 9 is not smaller than the average **grain size** of the polycrystal **semiconductor** film 3. The LCD device employing the TFT thus constructed is free from white spots...

...SPECIFICATION effect this accurate ON-OFF performance, it has been desirable that polycrystal silicon having a **grain size** as large as possible, e.g. 3 - 5 (mu)m, is used for the polycrystal **semiconductor** thin film, thereby to increase an ON-current of the TFT.
The market recently demands to improve the **picture** quality; however, the LCD device having a conventional TFT structure encounters a problem that a...

...illuminates brighter than a desired brightness, namely the micro

brighter spot looks whiter than other **pixels** .
This problem is conditioned by two reasons. One is that TFT has been progressively miniaturized...

...TFT shown in Fig. 4(b) employs silicon-made polycrystal semiconductor thin film of which **grain size** is 3 - 5 (mu)m as an active layer of the TFT. The progress of...

...low concentration region 4 of the source 6 and drain 7 becomes shorter than the **grain size** . In manufacturing the TFTs, impurity ion is implanted so that the low concentration region 4...
...low concentration region 4 substantially along the grain boundary 2. At this time, since the **grain size** is longer than the length "D" of the low concentration region 4, the high concentration...

...region measured from the edge of gate insulating film is not smaller than an average **grain size** of the polycrystal **semiconductor** thin film.
A manufacturing method of the TFT of the present invention comprises the following...from the edge of gate insulating film to at least a distance of an average **grain size** ,
(v) forming the source and the drain both having high impurity concentration by implanting the...

...been implanted.
The above structure and method provide polycrystal semiconductor film having a small average **grain size** . Therefore, even if the impurity diffuses from the high concentration region into the low concentration...

...set a length "D" of the low concentration region 4 not shorter than an average **grain size** of the polycrystal silicon film. For instance, an average **grain size** of polycrystal silicon film as the polycrystal **semiconductor** film 3 is controlled to be as fine as 1.0 (mu)m, and the ...

...CLAIMS concentration region from the edge of gate insulating film is not smaller than an average **grain size** of said polycrystal **semiconductor** thin film.
2. A thin film transistor manufacturing method comprising the steps of:
(i) forming...

...the edge of said gate insulating film to at least a distance of an average **grain size** ,
(v) forming said source and said drain both having high impurity concentration by implanting the...

20/3,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00997094
Semiconductor device having laser-annealed semiconductor elements, and display device using this semiconductor device
Halbleitervorrichtung mit lasergetemperten Halbleiterelementen sowie Anzeigevorrichtung, die diese Halbleitervorrichtung benutzt
Dispositif a semi-conducteur comportant des elements semi-conducteurs recuits par laser et dispositif d'affichage l'utilisant
PATENT ASSIGNEE:
SANYO ELECTRIC CO., LIMITED., (238925), 18 Keihan-Hondori 2-chome,

Moriguchi City, Osaka, (JP), (Applicant designated States: all)
INVENTOR:
Yoneda, Kiyoshi, 1495-6, Furuhashi, Sunami-cho, Motosu-gun, Gifu-ken, (JP)
Kihara, Katsuya, 1-4-1-302, Higashimachi, Ibukidai, Nishi-ku, Kobe-shi, Hyogo-ken, (JP)
LEGAL REPRESENTATIVE:
Cross, Rupert Edward Blount et al (42891), BOULT WADE TENNANT, Verulam Gardens 70 Gray's Inn Road, London WC1X 8BT, (GB)
PATENT (CC, No, Kind, Date): EP 901163 A2 990310 (Basic)
EP 901163 A3 010516
APPLICATION (CC, No, Date): EP 98307190 980907;
PRIORITY (CC, No, Date): JP 97243054 970908
DESIGNATED STATES: DE; FR; GB; NL
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: G02F-001/136; **H01L-027/12** ; G02F-001/1362; **H01L-021/84**
ABSTRACT WORD COUNT: 188
NOTE:
Figure number on first page: 9

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9910	1061
SPEC A	(English)	9910	7728
Total word count - document A			8789
Total word count - document B			0
Total word count - documents A + B			8789

...INTERNATIONAL PATENT CLASS: **H01L-027/12** ...

... **H01L-021/84**
...SPECIFICATION which a TFT is disposed as a switching element for controlling a timing for rewriting **image** data in each **pixel** , can display high-resolution animation in a large **image** plane, it is used in displays of various televisions, personal computers, and the like.
A...

...which has been frequently used, and annealing is performed using laser beams for formation or **growth** of p-Si crystal **grains** . In general, p-Si has a higher mobility compared with a-Si, a TFT is...

...a P-ch TFT, i.e. CMOS, can be formed, and a high-speed drive **circuit** can be constituted. Therefore, by forming a drive **circuit** area integrally with a display area on the same substrate, manufacturing cost can be reduced...

20/3,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00995514
Light emitting semiconductor device using nanocrystals
Lichtemittierende Halbleitervorrichtung, die Nanokristalle enthalt
Dispositif semi-conducteur emetteur de lumiere comprenant des nanocristaux
PATENT ASSIGNEE:
Toshiba Corporation, (213133), 72, Horikawa-cho, Saiwai-ku, Kawasaki-shi, Kanagawa-ken, (JP), (Applicant designated States: all)

INVENTOR:
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Kurobe, Atsushi, Toshiba Corp., Intel. Prop. Div., 1-1-1, Shibaura, Minato-ku Tokyo 105, (JP)
LEGAL REPRESENTATIVE:
Waldren, Robin Michael (55602), MARKS & CLERK, 57-60 Lincoln's Inn Fields , London WC2A 3LS, (GB)
PATENT (CC, No, Kind, Date): EP 899796 A2 990303 (Basic)
EP 899796 A3 010404
APPLICATION (CC, No, Date): EP 98306936 980828;
PRIORITY (CC, No, Date): JP 97234284 970829; JP 98178278 980625
DESIGNATED STATES: DE; FR; GB
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: **H01L-033/00** ; **H01L-027/15** ; **H01L-031/12**
ABSTRACT WORD COUNT: 137
NOTE:
Figure number on first page: 4

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9909	1091
SPEC A	(English)	9909	8833
Total word count - document A			9924
Total word count - document B			0
Total word count - documents A + B			9924

INTERNATIONAL PATENT CLASS: **H01L-033/00** ...

... **H01L-027/15** ...

... **H01L-031/12**

...ABSTRACT cause a quantum size effect. The microcrystals may be 10 nanometers (nm) or less in **grain size** . A dielectric film of 5 nm thick or less is formed containing therein such microcrystals. The microcrystal structure section is disposed between p- and n-type **semiconductor** layers. These layers are brought into electrical contact with the microcrystal structure only, while causing...

...SPECIFICATION degree)C for two minutes. The resultant Si microcrystals 12 are about 5 nm in **grain** diameter or **size** . Next, the structure is again oxidized in an oxygen gas at a temperature of 750...

...oxidation of the part of the structure around the microcrystals 12. In this way the **semiconductor** microcrystal layer 14 is fabricated to have the SiO2)) film 13 on the surface of...

...gas atmosphere at 500(degree)C for ten minutes, whereby the Si microcrystals 22 of **grain size** of several nanometers are formed within the silicon oxide film. The **grain size** of such Si microcrystals 22 are well controllable by adjustment of the heating time period 22 to thereby form the **semiconductor** microcrystal layer 24.

Then, both Si and Boron (B) dopants are supplied simultaneously to the ...invention. The flat-surface display panel includes a matrix array of rows and columns of **picture elements** or " **pixels** " each employing the pin-junction LED of Fig. 1.

As shown in Fig. 5. the...

20/3,K/6 (Item 6 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00891423
Solid state radiation detector
Festkorper-Strahlungsdetektor
Detecteur de radiation a l'etat solide
PATENT ASSIGNEE:
MINNESOTA MINING AND MANUFACTURING COMPANY, (300410), 3M Center, P.O. Box 33427, St. Paul, Minnesota 55133-3427, (US), (applicant designated states: DE;FR;GB;IT)
INVENTOR:
Tran, Nang, c/o Minnesota Mining & Manuf.Co. 2501 Hudson Road, PO Box 33427, Saint Paul, MN 55133-3427, (US)
LEGAL REPRESENTATIVE:
VOSSIUS & PARTNER (100314), Siebertstrasse 4, 81675 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 814503 A2 971229 (Basic)
EP 814503 A3 980930
APPLICATION (CC, No, Date): EP 97113907 930218;
PRIORITY (CC, No, Date): US 839268 920220
DESIGNATED STATES: DE; FR; GB; IT
RELATED PARENT NUMBER(S) - PN (AN):
EP 556820 (EP 931025472)
INTERNATIONAL PATENT CLASS: **H01L-021/336** ; **H01L-027/12** ; **H01L-027/146** ; **H01L-031/0232**
ABSTRACT WORD COUNT: 112

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9712W3	642
SPEC A	(English)	9712W3	4393
Total word count - document A			5035
Total word count - document B			0
Total word count - documents A + B			5035

INTERNATIONAL PATENT CLASS: **H01L-021/336** ...

... **H01L-027/12** ...

... **H01L-027/146** ...

... **H01L-031/0232**

...SPECIFICATION array 16 is fed to the electrodes of associated TFTs in the array 18.
The **pixels** forming such an array are typically 85(mu)m X 85(mu)m in area...

...with respect to the TFTs is essential for a commercially viable device that produces an **image** with satisfactory resolution. The greater the amount of defective **pixels** in such a device, the poorer the resolution of the **image** . In addition, alignment of the layers in each **pixel** results in an active area in each **pixel** that is greater than the active areas in **pixels** produced under prior art methods. The sequence of microlithographic steps that were used in prior...

...present invention automatically aligns the layers as discussed above,

the resulting active area of each **pixel** is greater.
An example of the process of the present invention that produces the sensing...or with cesium iodine doped with thallium. The phosphor may be situated individually over each **pixel** in microcolumns. The individual microcolumn arrangement confines the scattered emitted light to the area of the associated **pixel** . Although conventional screens can also be used with the present invention, the use of such...

...screen results in some spreading of the emitted light which causes a reduction in the **image** sharpness.
The use of columnar phosphor results in greater image sharpness since the emitted light...

...be formed by evaporating cesium iodine doped with thallium on the detector.
A metal-oxide- **semiconductor** field effect transistor (MOSFET) may be substituted for the thin film transistor to produce the...

...using furnace annealing, rapid thermal annealing, E-beam annealing, or laser annealing to form large **grain size** polycrystalline or single crystal silicon. The crystallized silicon layer is then patterned into islands using...

20/3,K/7 (Item 7 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00885991
Laser crystallisation of an amorphous silicon film for a TFT
Laserkristallisation eines amorphen Siliziumfilms fur einen TFT
Crystallisation laser d'une couche de silicium amorphe pour un TFT
PATENT ASSIGNEE:
Sanyo Electric Co., Ltd., (2206450), 5-5, Keihanhondori 2-chome, Moriguchi-shi, Osaka, (JP), (Proprietor designated states: all)
INVENTOR:
Yoneda, Kiyoshi, 1495-6 Furuhashi, Sunami-cho, Motosu-Gun, Gifu, (JP)
LEGAL REPRESENTATIVE:
Cross, Rupert Edward Blount et al (42891), BOULT WADE TENNANT, Verulam Gardens 70 Gray's Inn Road, London WC1X 8BT, (GB)
PATENT (CC, No, Kind, Date): EP 810639 A2 971203 (Basic)
EP 810639 A3 990728
EP 810639 B1 030416
APPLICATION (CC, No, Date): EP 97303681 970602;
PRIORITY (CC, No, Date): JP 96139206 960531
DESIGNATED STATES: DE; FR; GB; NL
INTERNATIONAL PATENT CLASS: **H01L-021/20** ; **H01L-021/336** ; G02F-001/136
ABSTRACT WORD COUNT: 146
NOTE:
Figure number on first page: 4

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199711W4	810
CLAIMS B	(English)	200316	723
CLAIMS B	(German)	200316	662
CLAIMS B	(French)	200316	907
SPEC A	(English)	199711W4	4441
SPEC B	(English)	200316	4500

Total word count - document A 5252
Total word count - document B 6792
Total word count - documents A + B 12044

INTERNATIONAL PATENT CLASS: **H01L-021/20** ...

... **H01L-021/336**

...SPECIFICATION matrix type provided with a TFT, as a switching element for controlling timings for rewriting **image** data on **pixels** , realizes motion animation display with a large screen and high resolution, and is therefore used...

...which had frequently been adopted has been developed, and annealing using a laser beam for **growth** of **grains** has been put to use. In general, p-Si has a higher mobility than a...

...be achieved. Consequently, an electrically complementary connection structure, e.g., a CMOS (Complementary Metal Oxide **Semiconductor**) can be constructed using an n-ch TFT and a p-ch TFT so that a high-speed drive **circuit** can be formed by adopting p-Si TFT. Since a driver **circuit** section can therefore be formed to be integral with a display area on the same...

...SPECIFICATION matrix type provided with a TFT, as a switching element for controlling timings for rewriting **image** data on **pixels** , realizes motion animation display with a large screen and high resolution, and is therefore used...

...which had frequently been adopted has been developed, and annealing using a laser beam for **growth** of **grains** has been put to use. In general, p-Si has a higher mobility than a...

...be achieved. Consequently, an electrically complementary connection structure, e.g., a CMOS (Complementary Metal Oxide **Semiconductor**) can be constructed using an n-ch TFT and a p-ch TFT so that a high-speed drive **circuit** can be formed by adopting p-Si TFT. Since a driver **circuit** section can therefore be formed to be integral with a display area on the same...

20/3,K/8 (Item 8 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00865964
Semiconductor device, display device with a semiconductor device, and production method thereof
Halbleiter, Display mit Halbleiter und seine Herstellung
Dispositif semi-conducteur, dispositif d'affichage avec des dispositifs semi-conducteurs et methode de fabrication associee
PATENT ASSIGNEE:
CANON KABUSHIKI KAISHA, (542361), 30-2, 3-chome, Shimomaruko, Ohta-ku, Tokyo, (JP), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
Okita, Akira, c/o Canon K.K., 30-2, 3-chome, Shimomaruko, Ohta-ku, Tokyo, (JP)
LEGAL REPRESENTATIVE:
Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. 2-5 Warwick Court High Holborn, London WC1R 5DJ, (GB)

PATENT (CC, No, Kind, Date): EP 795904 A2 970917 (Basic)
EP 795904 A3 980729
APPLICATION (CC, No, Date): EP 96306678 960913;
PRIORITY (CC, No, Date): JP 95236866 950914; JP 96241935 960912
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: **H01L-023/00** ; **H01L-023/31**
ABSTRACT WORD COUNT: 173

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9709W2	997
SPEC A	(English)	9709W2	6799
Total word count - document A			7796
Total word count - document B			0
Total word count - documents A + B			7796

INTERNATIONAL PATENT CLASS: **H01L-023/00** ...

... **H01L-023/31**

...SPECIFICATION has been an increasing need for a liquid crystal display device capable of displaying an **image** with higher resolution. Among various types, a liquid crystal display device of the active matrix type in which **pixels** are switched by thin film switching devices has been developed rapidly since a crosstalk occurs little even when the number of **pixels** is increased and a high-quality **image** with a high gradation can be easily achieved.

In active matrix type liquid crystal display...

...matrix type liquid crystal display device and Fig. 11B is an enlarged view of an **image** display unit thereof. In Fig. 11A, reference numeral 61 denotes a video signal circuit; 62...

...is a vertical shift register; 64 is a horizontal shift register; and 65 is an **image** display unit. In Fig. 11B, reference numerals 21a, 21b and 21c denote scanning interconnections; 22a...

...is a storage capacitance; 23 is a thin film transistor (TFT); and 28 is a **pixel** electrode. The video signal circuit 61 outputs a television signal to the horizontal shift register 64. The horizontal shift register 64 samples the television signal corresponding to each **pixel** of the **image** display unit 65. The vertical shift register 63 controls the timing of selecting a row of **image** display unit 65. The synchronizing circuit 62 controls the timing of the operation of vertical shift register 63 and horizontal shift register 64. In the **image** display unit shown in Fig. 11B, TFT 23, storage capacitor 20 and **pixel** electrode 28 are disposed at each intersection of the scanning interconnections 21a, 21b and 21c...

...The vertical shift register 63 outputs a row selection pulse which is supplied to the **image** display unit through the scanning interconnections 21a, 21b, and 21c. TFTs turn ON and OFF...

...response to row selection pulses. As a result a television signal is written in the **pixel** electrodes 28 and storage capacitors 20 through the data interconnections 22a, 22b, 22c, and 22d...

...shift register 64 as well as the TFTs are formed of polycrystalline silicon, wherein the **image** display unit 65, the vertical shift register 63 and the horizontal shift register 64 are...

...electrodes; 13 is a hydrogen supply layer; 14 is light blocking films; 16 is a **pixel** electrode; and 17 is a **pixel** display area. A scanning interconnection is connected to each gate electrode 8. In response to...

...turns ON. As a result, a signal on the data interconnection is applied to the **pixel** electrode 16 via the channel 9. In the present invention, the term "semiconductor layer" is...capacitor is formed with the light blocking film 14 disposed directly on the TFT, the **pixel** electrode 16 and the interlayer insulating film 15 disposed between them. In this invention, as...

...the case of the transmission type liquid crystal display device a greater size of the **pixel** display area 17 can be achieved. This makes it possible to realize a liquid crystal display device having a high opening ratio and thus capable of displaying a bright **image** . In contrast, in the liquid crystal display device according to the conventional technique shown in...suppressed to a low level. As a result, a charge can be held at the **pixel** electrode for a long time and thus it is possible to achieve a liquid crystal display device capable of displaying a high-contrast **image** . Furthermore, the display device includes a low density of defects such as white or black...

20/3,K/9 (Item 9 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00769997
A RADIATION DETECTION SYSTEM AND PROCESSES FOR PREPARING THE SAME
STRAHLUNGSEMPFANGSSYSTEM UND HERSTELLUNGSVERFAHREN
SYSTEME DE RADIODETECTION ET SON PROCEDE DE FABRICATION
PATENT ASSIGNEE:
DIRECT (Digital Imaging Readout), (3200330), c/o Yissum Research Development Company of the Hebrew Universitty of Jerusalem 46 Jabotinsky Street, Jerusalem 91042, (IL), (Proprietor designated states: all)
INVENTOR:
SCHIEBER, Michael, Misho, 9 Bartenura Street, 91204 Jerusalem, (IL)
NISSENBAUM, Jacob, Baruch, 4 Revadim Street, 93391 Jerusalem, (IL)
HAREL, Ze'ev, 8 Hatzedef Street, 40295 Hofit, (IL)
LEGAL REPRESENTATIVE:
Ablewhite, Alan James et al (27521), MARKS & CLERK, 57/60 Lincoln's Inn Fields, London WC2A 3LS, (GB)
PATENT (CC, No, Kind, Date): EP 784801 A1 970723 (Basic)
EP 784801 A1 980819
EP 784801 B1 020424
WO 9610194 960404
APPLICATION (CC, No, Date): EP 95935103 950929; WO 95US12222 950929
PRIORITY (CC, No, Date): IL 11108594 940929; IL 11353595 950428
DESIGNATED STATES: DE; ES; FR; GB; IE; IT; NL; SE
INTERNATIONAL PATENT CLASS: G01T-001/24; G01T-001/29; G01J-005/26; **H01L-031/032**
NOTE:
No A-document published by EPO
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200217	811
CLAIMS B	(German)	200217	799
CLAIMS B	(French)	200217	935

SPEC B (English) 200217 7414
Total word count - document A 0
Total word count - document B 9959
Total word count - documents A + B 9959

...INTERNATIONAL PATENT CLASS: **H01L-031/032**

...SPECIFICATION iodide films.
Thus, according to the present invention, there are provided large-area, coherent, continuous **semiconductor** films, preferably having an area of between 102)cm2) and 104)cm2), and a thickness...

...about 1-500 (mu)m, which can be partially or fully textured (50-100%), with **grain size** from 1 (mu)m to 5 mm.
The present invention also provides processes for the...which are large enough to allow room temperature operation without cryogenic cooling.
From the various **image** receptors shown in Table 2, it is obvious that the high Z and high Eg...

...the field of gamma ray camera using bulk detectors of HgI2)), using 8 by 8 **pixels** (C. Ortale, et al., Nucl. Inst. and Methods, Vol. 213, p. 95 (1983)) and progressing to a 32 by 32 **pixel** array (see, e.g., B.E. Patt, et al., Nucl. Inst, and Methods, Vol. 283, p. 215 (1989)) with a **pixel** size of 0.8x0.8 mm2) and a thickness of 2 mm, with interelement spacing...distinct areas:
a) Menu area
b) Gray scale image display
c) Spectrum (daughter window)
d) **Image** characteristics (total count; sum of all counts; maximum counts; value of brightest **pixel** ; multiple counts; number of counts where signals are present in two adjacent rows or columns...

...CLAIMS strips being arranged relative to each other to form a grid-like array.
11. An **image** receptor according to claim 10, wherein said upper and substrate layers are respectively patterned with vertical and horizontal conductive strips, to produce a cross-grid representing a **pixel** of about 20-200 (mu)m width and about 20-200 (mu)m length.
12...

...film is a thin film having a thickness of 1-500(mu)m.
15. An **image** receptor according to claim 8, wherein said electrode comprises a grid of top patterned electrode **pixels** of about 20-200(mu)m width and about 20-200(mu)m length, each **pixel** being individually connected to an imaging electronic system.
16. A process for the preparation of...
...CLAIMS autre de facon a former un reseau semblable a une grille.
11. Un recepteur d' **image** selon la revendication 10, dans lequel des motifs de rubans conducteurs verticaux et horizontaux sont respectivement definis dans les couches superieure et de substrat, pour produire une grille representant un **pixel** d'environ 20-200 (mu)m de largeur et d'environ 20-200 (mu)m...

...une pellicule mince ayant une epaisseur de 1-500 (mu)m.
15. Un recepteur d' **image** selon la revendication 8, dans lequel l'electrode comprend une grille de **pixels** d'electrode superieure, resultant d'une operation de definition de motif, d'environ 20-200 (mu)m de largeur et d'environ 20-200 (mu)m de longueur, chaque **pixel** etant connecte individuellement a un systeme electronique **imageur** .

16. Un procede pour la preparation d'une pellicule continue consistant essentiellement en un materiau...

20/3,K/10 (Item 10 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00752255
Method of forming polycrystalline semiconductor thin film
Verfahren zur Herstellung einer dunnen polykristallinen Halbleiterschicht
Procede pour former une couche mince en semi-conducteur polycristallin
PATENT ASSIGNEE:
SONY CORPORATION, (214021), 7-35 Kitashinagawa 6-chome Shinagawa-ku, Tokyo 141, (JP), (Proprietor designated states: all)
INVENTOR:
Minegishi, Masahiro, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP)
Ino, Masumitsu, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP)
Kunii, Masafumi, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP)
Urazono, Takenobu, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP)
Hayashi, Hisao, c/o Sony Corporation, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, (JP)
LEGAL REPRESENTATIVE:
Muller, Frithjof E., Dipl.-Ing. (8661), Patentanwalte MULLER & HOFFMANN, Innere Wiener Strasse 17, 81667 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 708479 A2 960424 (Basic)
EP 708479 A3 960911
EP 708479 B1 010404
APPLICATION (CC, No, Date): EP 95116366 951017;
PRIORITY (CC, No, Date): JP 94280097 941019
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: **H01L-021/20** ; **H01L-021/336** ; **H01L-021/84**
ABSTRACT WORD COUNT: 180
NOTE:
Figure number on first page: 1A

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	682
CLAIMS B	(English)	200114	615
CLAIMS B	(German)	200114	582
CLAIMS B	(French)	200114	731
SPEC A	(English)	EPAB96	3786
SPEC B	(English)	200114	2179
Total word count - document A			4469
Total word count - document B			4107
Total word count - documents A + B			8576

INTERNATIONAL PATENT CLASS: **H01L-021/20** ...

... **H01L-021/336** ...

... **H01L-021/84**

...ABSTRACT A3

performing a first working operation in such a way that TFTs are formed while using said polycrystalline **semiconductor** thin film as an active layer of the TFTs;

performing a second working operation in...

...CLAIMS on an insulating substrate to form a precursory polycrystalline film comprising clusters of microscopic crystal **grains** wherein said **semiconductor** layer **growing** step is carried out at a temperature of 500 - 650(degree)C by CVD; and...

...a single-shot of a laser pulse energy beam to the precursory film to increase **grain size** of said crystal **grains** , thereby converting said precursory film into a polycrystalline **semiconductor** thin film, wherein the cross section of the laser pulse energy beam has the shape...

...layer on an insulating substrate to form a polycrystalline film comprising clusters of microscopic crystal **grains** wherein said step of **growing** said **semiconductor** layer is carried out at a film formation temperature of 500 - 650(degree)C by...

...a single-shot of a laser pulse energy beam to the polycrystalline film to increase **grain sizes** of said crystal **grains** and to convert said polycrystalline film into a polycrystalline **semiconductor** thin film, wherein the cross section of the laser pulse energy beam has the shape...

...on an insulating substrate to form a polycrystalline film comprised of clusters of microscopic crystal **grains** wherein said step of **growing** said **semiconductor** layer is carried out at a film formation temperature of 500 - 650(degree)C by...

...a single-shot of a laser-pulse energy beam to said polycrystalline film to increase **grain sizes** of said crystal **grains** and to convert said polycrystalline film into a polycrystalline **semiconductor** thin film, wherein the cross section of the laser pulse energy beam has the shape...

20/3,K/11 (Item 11 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00748209

METHOD OF MANUFACTURING A SEMICONDUCTOR THIN FILM TRANSISTOR
VERFAHREN ZUR HERSTELLUNG EINES DUNNSCHICHT-HALBLEITER-TRANSISTORS
PROCEDE DE FABRICATION D'UN TRANSISTOR SEMI-CONDUCTEUR A COUCHE MINCE

PATENT ASSIGNEE:
SEIKO EPSON CORPORATION, (730004), 4-1, Nishishinjuku 2-chome, Shinjuku-ku, Tokyo 163-0811, (JP), (Proprietor designated states: all)
INVENTOR:
MIYASAKA, Mitsutoshi, Seiko Epson Corporation 3-5, Owa 3-chome Suwa-shi, Nagano-ken 392, (JP)
LEGAL REPRESENTATIVE:
Hoffmann, Eckart, Dipl.-Ing. (5571), Patentanwalt, Bahnhofstrasse 103, 82166 Grafelfing, (DE)

PATENT (CC, No, Kind, Date): EP 714140 A1 960529 (Basic)
EP 714140 A1 980401
EP 714140 B1 030903

WO 95034916 951221
APPLICATION (CC, No, Date): EP 95921972 950615; WO 95JP1196 950615
PRIORITY (CC, No, Date): JP 94133374 940615; JP 9572144 950329
DESIGNATED STATES: CH; DE; FR; GB; IT; LI; NL; SE
RELATED DIVISIONAL NUMBER(S) - PN (AN):
EP 1335419 (EP 2003008849)
INTERNATIONAL PATENT CLASS: **H01L-021/205** ; G02F-001/136; **H01L-021/336** ; **H01L-021/20** ; C23C-016/24
ABSTRACT WORD COUNT: 133
NOTE:
Figure number on first page: 1D

LANGUAGE (Publication,Procedural,Application): English; English; Japanese
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	3903
CLAIMS B	(English)	200336	438
CLAIMS B	(German)	200336	401
CLAIMS B	(French)	200336	450
SPEC A	(English)	EPAB96	27200
SPEC B	(English)	200336	26937
Total word count - document A			31110
Total word count - document B			28226
Total word count - documents A + B			59336

INTERNATIONAL PATENT CLASS: **H01L-021/205** ...
... **H01L-021/336** ...

... **H01L-021/20**

...SPECIFICATION such as silicon spreads readily over the underlevel protection layer. Because of this, large diameter **grains** can **grow** easily; and the properties of the thin film **semiconductor** device are improved dramatically. At the same time, local agglomeration of the molten material during solidification of the melted **semiconductor** material does not occur; and the uniformity within the molten region increases. The LSI scaling law applies to thin film **semiconductor** devices as well; and it appears that the miniaturization of elements will continue in step...submicron order, how to avoid local agglomeration will be an important issue. When fabricating the **semiconductor** layer by melt crystallization, the center line mean surface roughness of the underlevel protection layer...

...By meeting this criterion, it is possible to produce uniform films, without local agglomeration, from **semiconductor** films with large-diameter grains.

Another role of the underlevel protection layer is to prevent...the presence of the many nuclei resulting from the outgassing will result in the average **grain size** of the crystallized film being small and cause a degradation in the transistor properties. Additionally, the trapping of outgassing impurities in the **semiconductor** film during growth leads to further decline in transistor properties. As explained in section (2...

...in suppressing the generation of nuclei. At the same time, the deposition conditions of the **semiconductor** film must also be carefully controlled. Consequently, in addition to the regulation of the surface... of 0.19 nm/min showed black spots throughout transmission electron micrographs and had small **grain sizes** following crystallization by RTA. As a result, the mobilities were also low when these films...10(sup

current. Having a sufficiently small optical leakage current is a condition for a good thin film **semiconductor** device. In the case of the thin film **semiconductor** device of this invention, the optical leakage current is proportional to the film thickness. From...off state leakage and optical leakage are important, such as when using a thin film **semiconductor** device for the pixel switching element of an LCD, it is desirable to have a **semiconductor** film thickness from 10 nm to 70 nm. Moreover, when it is necessary to give...

...carry out activation in a stable manner, a lower limit must be set for the **semiconductor** film thickness. With this invention, the desired value is 30 nm or higher. If an...

...utilized, a thickness of 50 nm or higher is desired.

2-14. Crystallization of the **Semiconductor** Film through VHF-PECVD and Microwave PECVD

As described in detail in section (2-12...At the same time, because the a-Si layer is composed of large regions, the **size** of the **grains** after crystallization is large and high-performance electrical characteristics can be obtained. In other words...matrix liquid crystal display device (LCD), high-definition LCDs (LCDs having a large number of **picture elements**), bright LCDs (LCDs having a high aperture ratio in which storage capacitors have been reduced or eliminated), and highly-integrated LCDs (LCDs having a large number of **picture elements** per unit area), all of which were heretofore impossible using a-Si TFTs of the...

20/3,K/12 (Item 12 from file: 348)

00719903

Method of processing a thin film on a substrate for display.

Verarbeitungsvorrichtung von einem dunnen Film uber einem Substrat fur eine Anzeige.

Procede de traitement d'un film mince sur un substrat pour dispositif d'affichage.

PATENT ASSIGNEE:
SONY CORPORATION, (214022), 7-35, Kitashinagawa 6-chome Shinagawa-ku, Tokyo, (JP), (applicant designated states: DE;FR;GB)
INVENTOR:
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LEGAL REPRESENTATIVE:
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PATENT (CC, No, Kind, Date): EP 681316 A2 951108 (Basic)
EP 681316 A3 980107

APPLICATION (CC, No, Date): EP 95106505 950428;
PRIORITY (CC, No, Date): JP 94116007 940502; JP 94257616 940927
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: **H01L-021/20**
ABSTRACT WORD COUNT: 158

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB95	625
SPEC A	(English)	EPAB95	10404
Total word count - document A			11029
Total word count - document B			0
Total word count - documents A + B			11029

INTERNATIONAL PATENT CLASS: **H01L-021/20**

...ABSTRACT out to form integrated thin film transistors on a sectioned area for one chip. Thereafter, **pixel** electrodes for one **picture** (frame) are formed within the sectioned area. During the series of processes, a laser pulse...

...doped in the semiconductor thin film can be performed by the batch heat treatment. (see **image** in original document)

...SPECIFICATION 1 is a schematic diagram showing a previous paper suggested laser beam irradiation method. A **semiconductor chip** 101 for display which is a target to be processed has such a laminating structure that a **semiconductor** thin film 103 is formed on a transparent insulating substrate 102. In this method, a...

...beam 105 is irradiated onto a predetermined sectioned area 104 which is provided on the **semiconductor** thin film 103. In the conventional method, the output power of the laser beam is...

...is limited to a narrow area about 100(mu)m(sup 2). Accordingly, when a **semiconductor** thin film 103 having a large area is required to be processed to satisfy a requirement for a large-scale picture, the laser beam is irradiated onto the whole **semiconductor** thin film while scanning the laser beam 105 or shifting the laser-irradiation area stepwisely...

...than to narrow the laser-irradiation area down. With increase of the energy density, a **semiconductor** thin film of amorphous silicon or polycrystal silicon having relatively small **grain size** is perfectly melted to increase its **grain size** . In this method, however, an irradiation time per **chip** increases and thus a throughput is reduced. Furthermore, the scanning of the irradiation of the...

...beam causes temperature difference to occur locally, and thus causes increase in dispersion of crystal **grain size** . Therefore, there occurs great dispersion in electrical characteristics of the thin film transistors such as...

...thin film transistors in a sectioned area for one chip and a step of forming **pixel** electrodes in the sectioned area to form a **picture** (frame), wherein the processing step contains a step of irradiating a laser pulse to the...

...the semiconductor thin film is melted to be recrystallized or annealed

crystallinity of the **semiconductor** thin film cannot be uniform over the same sectioned area. If a transistor is formed of such a **semiconductor** thin film having ununiform crystallinity as described above, dispersion in TFT's characteristics would occur in the same **chip** due to the different in **grain size** . In order to avoid such a disadvantage is proposed a method of selectively forming an...

...area. However, this method needs a process of beforehand forming an antireflection film on the **semiconductor** thin film by the patterning treatment, and thus it induces increase in the number of...of the laser pulse. Therefore, the semiconductor thin film can be perfectly melted, and the **grain size** of crystals can be easily increased.
According to the present invention, the one-shot irradiation...

...CLAIMS to form integrated thin film transistors in a sectioned area for one chip; and
forming **pixel** electrodes in the sectioned area to form a **picture** , wherein said processing step contains a step of irradiating a laser pulse to the sectioned...

20/3,K/13 (Item 13 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00573501
Semiconductor device.
Halbleitervorrichtung.
Dispositif a semi-conducteur.
PATENT ASSIGNEE:
SEIKO INSTRUMENTS INC., (839490), 31-1, Kameido 6-chome Koto-ku, Tokyo 136, (JP), (applicant designated states: DE;FR;GB)
INVENTOR:
Iwaki, Tadao, c/o Seiko Instruments Inc., 31-1 Kameido 6-chome, Koto-ku, Tokyo, (JP)
Yamazaki, Tsuneo, c/o Seiko Instruments Inc., 31-1 Kameido 6-chome, Koto-ku, Tokyo, (JP)
Matsushita, Katsuki, c/o Seiko Instruments Inc., 31-1 Kameido 6-chome, Koto-ku, Tokyo, (JP)
Senbonmatsu, Shigeru, c/o Seiko Instruments Inc., 31-1 Kameido 6-chome, Koto-ku, Tokyo, (JP)
Takano, Ryuichi, c/o Seiko Instruments Inc., 31-1 Kameido 6-chome, Koto-ku, Tokyo, (JP)
LEGAL REPRESENTATIVE:
Sturt, Clifford Mark et al (50502), J. MILLER & CO. 34 Bedford Row Holborn, London WC1R 4JH, (GB)
PATENT (CC, No, Kind, Date): EP 570224 A2 931118 (Basic)
EP 570224 A3 980311
APPLICATION (CC, No, Date): EP 93303709 930513;
PRIORITY (CC, No, Date): JP 92122024 920514
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: **H01L-021/76** ; **H01L-027/12** ; **H01L-027/14** ; G02F-001/136; G06E-003/00; **H01L-021/20**
ABSTRACT WORD COUNT: 138

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	1022
SPEC A	(English)	EPABF1	8957

Total word count - document A 9979
Total word count - document B 0
Total word count - documents A + B 9979

INTERNATIONAL PATENT CLASS: **H01L-021/76** ...

... **H01L-027/12** ...
... **H01L-027/14** ...

... **H01L-021/20**

...SPECIFICATION etching to process the single crystal silicon wafer to a predetermined thickness.

However, in conventional **semiconductor** thin film elements using amorphous or polycrystalline silicon thin film sub-micron transistor elements cannot be formed by applying fine **semiconductor** manufacturing techniques. For example, as the amorphous silicon thin film is formed at a temperature...

...cannot be carried out. Furthermore, as polycrystalline silicon thin film, which is used for a **semiconductor** thin film element, has a crystalline **grain size** of several (mu)m it is limited naturally to miniaturise a thin film element. As...The semiconductor circuit elements in the integrated circuit chip 26 include a matrix in a **pixel** region 29, an X-driver in a side region 27, and a Y-driver in a side region 28. The matrix in the **pixel** region 29 is formed of fine **pixel** electrodes and integrated gate field effect transistors corresponding to the fine **pixel** electrodes, or of PN type **photo** diodes. The X-driver in the side region 27 is formed of drive circuits for supplying electrical signals to the respective transistors or **photo** diodes. The Y-driver in the side region 28 is formed of drive circuits acting...

...circuits for scanning sequentially the respective transistors or for scanning and detecting sequentially the respective **photo** diodes. As the single crystal thin film has a higher mobility than that of an...

...response characteristics can be formed on the same surface together with the matrix in the **pixel** region.

A portion 30 (Fig. 9) of an optical detector array is illustrated diagrammatically and...liquid crystal light valve 75. Each liquid crystal light valve includes a matrix in a **pixel** region of approximately 20 x 20 mm, of 480 x 720 **pixels** , each with a **pixel** electrode of approximately 18 x 20 (mu)m. The liquid crystal light valve device employs...

...layer as liquid crystal material and has a contrast ratio of 50 to 100. An **image** is driven in response to video signals from a first liquid crystal device drive circuit 65 and a second liquid crystal device drive circuit 72. The **image** of an object 63 taken by a CCD camera 64 is combined with a reference **image** from an **image** memory 66 by means of the first liquid crystal device drive circuit 65 to display the outcome on the first liquid crystal device 69. The **image** of the object 63 appears as an input **image** 78 (Fig. 19) and the reference **image** as a reference **image** 79. The object 63 is a Chinese character "Hikari" in Mincyotai type and the reference **image** is a Chinese character "Hikari" in Gothic type. The **images** are displayed side by side on the first liquid crystal device 60.

The input image...The thin film makes it possible to form a liquid crystal light valve with fine **pixels** and a large number of **pixels** , or to form an optical detector with good light transparency. Hence it is

possible to display and measure fine **images** .
In one embodiment of semiconductor thin film element manufacturing method according to the present invention...

...valve employing the semiconductor thin film element can be a liquid crystal display device with **pixels** each having a 5 to 20 m square near to a light wavelength. As a conventional coherent light-using display can provide **image** quality analogous to that of **photographic** film, the liquid crystal display device contributes largely and technically to a high resolution display...

...possible to miniaturise and provide higher resolution power of the optical correlation device. Furthermore, the **pixel** with a size near to light wavelength may be applied to a multi-filter type...

20/3,K/14 (Item 14 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00569328
Manufacturing electronic devices comprising, e.g., TFTs and MIMs.
Herstellung von elektronischen Anordnungen, die zum Beispiel TFTs und MIMs enthalten.
Fabrication de dispositifs electroniques comportant entre autre TFTs et MIMs.
PATENT ASSIGNEE:
PHILIPS ELECTRONICS UK LIMITED, (215204), 420-430 London Road, Croydon CR9 3QR, (GB), (applicant designated states: GB)
Koninklijke Philips Electronics N.V., (200769), Groenewoudseweg 1, 5621 BA Eindhoven, (NL), (applicant designated states: DE;FR;IT;NL)
INVENTOR:
Shannon, John Martin, c/o Philips Research Lab., Cross Oak Lane, Redhill, Surrey RH1 5HA, (GB)
LEGAL REPRESENTATIVE:
Stevens, Brian Thomas et al (36361), PHILIPS ELECTRONICS Patents and Trade Marks Department Philips House 1-19 Torrington Place, London WC1E 7HD, (GB)
PATENT (CC, No, Kind, Date): EP 561462 A2 930922 (Basic)
EP 561462 A3 941019
APPLICATION (CC, No, Date): EP 93200730 930312;
PRIORITY (CC, No, Date): GB 9206086 920320
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: **H01L-021/336** ; **H01L-021/20** ; **H01L-021/3105** ; **H01L-021/84**
ABSTRACT WORD COUNT: 229

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	631
SPEC A	(English)	EPABF1	5731
Total word count - document A			6362
Total word count - document B			0
Total word count - documents A + B			6362

INTERNATIONAL PATENT CLASS: **H01L-021/336** ...

... **H01L-021/20** ...

... **H01L-021/3105** ...

... **H01L-021/84**

...ABSTRACT be retained for that purpose. This permits the fabrication of an LCD device comprising a **picture - element** array of MIM type devices in the unconverted material (32) of the layer and TFT driver circuitry in the crystalline silicon material (36) of the layer. (see **image** in original document) (see **image** in original document)

...SPECIFICATION used as the switching devices in an array for actively controlling the operation of the **picture elements** of a liquid-crystal display. In more recent years MIM-type devices have been used...987 (our reference PHB33417). The device has a row and column matrix array of individual **picture elements** 10, only a few of which are shown in Figure 1 for simplicity. In practice...

...example of glass or other low-cost insulating material) with liquid-crystal material therebetween. The **picture - element** array is located over the main central area of the substrates, whereas driving circuits 28...

...together in rows and columns. Each individual electrode 18 defines the area of a respective **picture element** 10. The substrate 14 also carries a switching array of MIM devices 24 (integrated with the **picture - element** electrodes 18), a set of parallel row-address conductors 22, and row-driver circuitry 28...

...address conductors 20 extend at right angles to the row conductors 22. Where they overlie **picture - element** electrodes 18, the conductors 20 constitute the other electrodes of the **picture elements** 10.

The **picture - element** electrodes 18 of all **picture elements** in the same row are connected to a respective row-address conductor 22 (Figures 1...

...the form of MIM devices 24. Although only one MIM device is shown for each **picture element** , two or more MIM devices 24 could be associated with each **picture element** 10 in known manner.

The individual picture elements 10 are addressed in conventional fashion using...18, the chromium area 18a is exposed and is now etched away so that this **picture - element** area becomes transparent.

A further photolithographic and etching stage is then carried out to provide...

...insulating material 32 with the laser beam 40 is of surprisingly good quality for producing **semiconductor** devices, in spite of the material 32 having been deposited at a low temperature. Spectroscopy measurements show that polycrystalline silicon material of large **grain size** is produced.

In a particular example an amorphous non-stoichiometric silicon nitride material 32 formed...

20/3,K/15 (Item 15 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00562763
Process for producing a solid state radiation detector.
Verfahren zur Herstellung eines Festkorperstrahlungsdetektors.

Procede pour produire un detecteur de rayonnement a l'etat solide.

PATENT ASSIGNEE:
MINNESOTA MINING AND MANUFACTURING COMPANY, (300410), 3M Center, P.O. Box 33427, St. Paul, Minnesota 55133-3427, (US), (applicant designated states: DE;FR;GB;IT)
INVENTOR:
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VOSSIUS & PARTNER (100311), Postfach 86 07 67, D-81634 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 556820 A1 930825 (Basic)
APPLICATION (CC, No, Date): EP 93102547 930218;
PRIORITY (CC, No, Date): US 839268 920220
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: **H01L-021/336** ; **H01L-027/12**
ABSTRACT WORD COUNT: 118

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	1278
SPEC A	(English)	EPABF1	4423
Total word count - document A			5701
Total word count - document B			0
Total word count - documents A + B			5701

INTERNATIONAL PATENT CLASS: **H01L-021/336** ...

... **H01L-027/12**

...SPECIFICATION array 16 is fed to the electrodes of associated TFTs in the array 18.
The **pixels** forming such an array are typically 85(mu)m X 85(mu)m in area...

...with respect to the TFTs is essential for a commercially viable device that produces an **image** with satisfactory resolution. The greater the amount of defective **pixels** in such a device, the poorer the resolution of the **image** . In addition, alignment of the layers in each **pixel** results in an active area in each **pixel** that is greater than the active areas in **pixels** produced under prior art methods. The sequence of microlithographic steps that were used in prior...

...present invention automatically aligns the layers as discussed above, the resulting active area of each **pixel** is greater.
An example of the process of the present invention that produces the sensing...or with cesium iodine doped with thallium. The phosphor may be situated individually over each **pixel** in microcolumns. The individual microcolumn arrangement confines the scattered emitted light to the area of the associated **pixel** . Although conventional screens can also be used with the present invention, the use of such...

...screen results in some spreading of the emitted light which causes a reduction in the **image** sharpness.
The use of columnar phosphor results in greater image sharpness since the emitted light...

...be formed by evaporating cesium iodine doped with thallium on the detector.
A metal-oxide- **semiconductor** field effect transistor (MOSFET) may be

substituted for the thin film transistor to produce the...
...produce the MOSFET using the process of the present invention, the substrate (which is silicon **wafer** coated with 1-3(mu)m of thermal oxide for insulating) is coated with an...

...using furnace annealing, rapid thermal annealing, E-beam annealing, or laser annealing to form large **grain size** polycrystalline or single crystal silicon. The crystallized silicon layer is then patterned into islands using...

20/3,K/16 (Item 16 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00480082
Solid state X-ray imaging device
Rontgen-Abbildungsvorrichtung aus Festkorperbauelementen
Dispositif a l'etat solide d'imagerie par rayons X
PATENT ASSIGNEE:
MINNESOTA MINING AND MANUFACTURING COMPANY, (300410), 3M Center, P.O. Box 33427, St. Paul, Minnesota 55133-3427, (US), (applicant designated states: BE;CH;DE;FR;GB;IT;LI;NL;SE)
INVENTOR:
Tri Tran, Nang, c/o Minnesota Mining and, Manufact. Co., 2501 Hudson Road, P.O. Box 33427, St. Paul, Minnesota 55133-3427, (US)
Dahlquist, John C., c/o Minnesota Mining and, Manufact. Co., 2501 Hudson Road, P.O. Box 33427, St. Paul, Minnesota 55133-3427, (US)
LEGAL REPRESENTATIVE:
Molyneaux, Martyn William et al (34016), c/o Ladas & Parry, 52-54 High Holborn, London WC1V 6RR, (GB)
PATENT (CC, No, Kind, Date): EP 441521 A1 910814 (Basic)
EP 441521 B1 970528
APPLICATION (CC, No, Date): EP 91300700 910130;
PRIORITY (CC, No, Date): US 478201 900209
DESIGNATED STATES: BE; CH; DE; FR; GB; IT; LI; NL; SE
INTERNATIONAL PATENT CLASS: **H01L-027/146** ; **H01L-031/0232** ; **H01L-031/115** ; **H01L-031/14**
ABSTRACT WORD COUNT: 114

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	255
CLAIMS B	(English)	EPAB97	598
CLAIMS B	(German)	EPAB97	594
CLAIMS B	(French)	EPAB97	692
SPEC A	(English)	EPABF1	4688
SPEC B	(English)	EPAB97	4791
Total word count - document A			4943
Total word count - document B			6675
Total word count - documents A + B			11618

INTERNATIONAL PATENT CLASS: **H01L-027/146** ...

... **H01L-031/0232** ...

... **H01L-031/115** ...
... **H01L-031/14**

...SPECIFICATION at approximately 620(degree)C for 24 hours to form a crystalline polysilicon layer. The **grain size** of the crystalline polysilicon ranged from 500A - 3,000A.
The now crystalline polysilicon layer was...

...SPECIFICATION of U.S. Patents 4,689,487 and 4,810,881 has a non-destructive **image** read-out capability.

EP-A-0028960 discloses a detector comprising a plurality of **pixels** which each comprise a photodiode conductively connected to a gate of a thin film transistor...

...a thin film transistor employing amorphous silicon in which the transistors are used for optical **image** sensors in an **image** scanner.

SUMMARY OF THE INVENTION
According to this invention there is provided a radiation detector... chemical vapor deposition could also have been used to form the polysilicon amorphous layer.
The **wafers** containing the two layers were then annealed in a nitrogen atmosphere of approximately 200 Pa...

...at approximately 620(degree)C for 24 hours to form a crystalline polysilicon layer. The **grain size** of the crystalline polysilicon ranged from 500x10-10) - 3000 x 10-10) m (500A - 3...

20/3,K/17 (Item 17 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00459530
Method of forming crystals.
Verfahren zur Herstellung von Kristallen.
Methode pour former des cristaux.
PATENT ASSIGNEE:
CANON KABUSHIKI KAISHA, (542361), 30-2, 3-chome, Shimomaruko, Ohta-ku, Tokyo, (JP), (applicant designated states: AT;BE;CH;DE;DK;ES;FR;GB;GR;IT;LI;LU;NL;SE)
INVENTOR:
Sato, Nobuhiko, c/o CANON KABUSHIKI KAISHA, 3-30-2, Shimomaruko, Ohta-ku, Tokyo, (JP)
LEGAL REPRESENTATIVE:
Buhling, Gerhard, Dipl.-Chem. et al (2644), Patentanwaltsburo Tiedtke-Buhling-Kinne & Partner Bavariaring 4, D-80336 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 455981 A1 911113 (Basic)
APPLICATION (CC, No, Date): EP 91105269 910403;
PRIORITY (CC, No, Date): JP 9090442 900406; JP 9189118 910329
DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FR; GB; GR; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS: **H01L-021/20** ; C30B-025/18
ABSTRACT WORD COUNT: 207
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	219
SPEC A	(English)	EPABF1	7422
Total word count - document A			7641
Total word count - document B			0
Total word count - documents A + B			7641

INTERNATIONAL PATENT CLASS: **H01L-021/20** ...

...SPECIFICATION oxides and silicon nitrides are stable amorphous materials, which have been widely used for silicon **integrated circuit** processing. Such amorphous compounds are formed by chemical vapor deposition. When silicon was deposited on...

...amorphous layer or at best, a polycrystalline silicon layer, was formed with a variety of **grain sizes** . That is because the silicon layer was formed by spontaneous nucleation, coalescence and recrystallization. In ...of large area semiconductor devices such as solar batteries or switching transistors of liquid crystal **picture elements** , etc, in which devices are arranged in an array on a cheap glass, are becoming...

...etc.
On the other hand, the method for forming a polycrystalline thin film with great **grain sizes** by melting and solidification had problems. A great deal of time is required to form...

...due to scanning of amorphous or single crystal thin film with energy beam for every **wafer** . Therefore, that technique is poor in bulk productivity, and also, it is not suited for...
...if a continuous thin film may be formed, it has a polycrystalline structure with great **grain size** distribution and is difficult to apply for **semiconductor** devices.
Also, as long as a diamond substrate is used, it is expensive as a...

20/3,K/18 (Item 18 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00315792
Method for forming semiconductor crystal and semiconductor crystal article obtained by said method.
Verfahren zur Herstellung eines Halbleiterkristalls und dabei hergestellter Halbleiterkristall.
Methode pour former un cristal semi-conducteur et cristal semi-conducteur produit par cette methode.
PATENT ASSIGNEE:
CANON KABUSHIKI KAISHA, (542361), 30-2, 3-chome, Shimomaruko, Ohta-ku Tokyo, (JP), (applicant designated states: AT;BE;CH;DE;ES;FR;GB;GR;IT;LI;LU;NL;SE)
INVENTOR:
Yamagata, Kenji, 10-1, Asahi-cho 2-chome, Atsugi-shi Kanagawa-ken, (JP)
Kumomi, Hideya, 1-5, Aoto 5-chome Katsushika-ku, Tokyo, (JP)
Tokunaga, Hiroyuki, 10-6-402, Nanpeidai Miyamae-ku, Kawasaki-shi Kanagawa-ken, (JP)
Arao, Kozo, Paresusaido Jyoto 401 1-17, Sawa-cho, Hikone-shi Shiga-ken, (JP)
LEGAL REPRESENTATIVE:
Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. 2-5 Warwick Court High Holborn, London WC1R 5DJ, (GB)
PATENT (CC, No, Kind, Date): EP 307109 A1 890315 (Basic)
APPLICATION (CC, No, Date): EP 88307842 880824;
PRIORITY (CC, No, Date): JP 87209456 870824
DESIGNATED STATES: AT; BE; CH; DE; ES; FR; GB; GR; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS: **H01L-021/20** ; C30B-025/18
ABSTRACT WORD COUNT: 91

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	2661
SPEC A	(English)	EPABF1	7295
Total word count - document A			9956
Total word count - document B			0
Total word count - documents A + B			9956

INTERNATIONAL PATENT CLASS: **H01L-021/20** ...

...SPECIFICATION THE INVENTION
Field of the Invention
This invention relates to a method for forming a **semiconductor** crystal and a **semiconductor** crystal article obtained by said method, particularly to a method for forming a **semiconductor** single crystal or a **semiconductor** polycrystal controlled in **grain size** prepared by utilizing the difference in nucleation density of the deposited materials according to the...

...of large area semiconductor devices such as solar batteries of switching transistors of liquid crystal **picture elements** , etc., in which devices are arranged in an array on a cheap glass are becoming... etc.
On the other hand, the method for forming a polycrystalline thin film with great **grain sizes** by melting and solidification had the problems that an enormous time is required due to scanning of amorphous or single crystal thin film with energy beam for every **wafer** to be poor in bulk productivity, and also that it is not suited for enlargement...

...if a continuous thin film may be formed, it has a polycrystalline structure with great **grain size** distribution and can be difficultly applied for **semiconductor** device.
Also, as long as a diamond substrate is used, it is expensive as a... all on the thin film 5, as already mentioned.
The island-shaped semiconductor single crystal **grain** 7 further **grows** while maintaining the single crystal structure with the nucleation surface (S(sub(NDL))) 6 as single crystal **grains** 13-1, 13-2 further **grow** to becomes **semiconductor** single crystals 13A-1, 13A-2 until the adjacent **semiconductor** single crystals 13A-1, 13A-2 contact each other as shown in Fig. 7C, but...

...all on the thin film 5A, as already mentioned.
The island-shaped semiconductor single crystal **grain** 7 further **grows** while maintaining the single crystal structure with the nucleation surface (S(sub(NDL))) 6A as...

...cover over the whole surface of the thin film 5 as shown in Fig. 10C (**semiconductor** single crystal 7A).
Subsequently, if necessary, the semiconductor single crystal 7A is flattened by etching...the surface plane in amorphous surface is not determined.
The island-shaped semiconductor single crystal **grains** 13-1, 13-2 further **grow** to become **semiconductor** single crystals 13A-1, 13A-2 until the adjacent **semiconductor** single crystals 13A-1, 13A-2 contact each other as shown in Fig. 7C, but...pressure of 150 Torr. The i-silicon monocrystals grow until they mutually collide, thus forming **grain** boundaries 1508. The **grown** crystals show characteristic facets as shown in Fig. 19. The photovoltaic device shows, under the...

...light, for example, electric characteristics of an open-end voltage of 0.62V, a short- **circuit** current of 32 mA/cm(sup 2), and a fill factor of 0.8.
The...

...grown from the silicon monocrystal seeds generated only on the Mo film 2001, and the **growth** is terminated when the **grain size** reaches 5 - 6 (mu)m. In the following there is shown an example of crystal...

20/3,K/19 (Item 19 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00315219
Method for growth of crystal.
Verfahren zum Zuchten eines Kristalls.
Methode pour la croissance d'un cristal.
PATENT ASSIGNEE:
CANON KABUSHIKI KAISHA, (542361), 30-2, 3-chome, Shimomaruko, Ohta-ku, Tokyo, (JP), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
Yonehara, Takao, 2235-2, Nurumizu, Atsugi-shi Kanagawa-ken, (JP)
Yamagata, Kenji, 10-1, Asahi-cho 2-chome, Atsugi-shi Kanagawa-ken, (JP)
Nishigaki, Yuji, 893-19, Odake, Odawara-shi Kanagawa-ken, (JP)
LEGAL REPRESENTATIVE:
Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. 2-5 Warwick Court High Holborn, London WC1R 5DJ, (GB)
PATENT (CC, No, Kind, Date): EP 306153 A1 890308 (Basic)
EP 306153 B1 950322
APPLICATION (CC, No, Date): EP 88307262 880805;
PRIORITY (CC, No, Date): JP 87198690 870808
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: **H01L-021/20** ; C30B-025/18
ABSTRACT WORD COUNT: 112

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	376
CLAIMS B	(English)	EPAB95	368
CLAIMS B	(German)	EPAB95	364
CLAIMS B	(French)	EPAB95	417
SPEC A	(English)	EPABF1	3465
SPEC B	(English)	EPAB95	3473
Total word count - document A			3841
Total word count - document B			4622
Total word count - documents A + B			8463

INTERNATIONAL PATENT CLASS: **H01L-021/20** ...

...SPECIFICATION years about large area semiconductor devices such as solar battery, switching transistor of liquid crystal **picture element** , etc. in which devices are arranged in an array on an inexpensive glass.
What is...photoelectric transducing device, etc.
Also, the method for forming a polycrystalline thin film with greater **grain size** by melting and solidification has involved the problems such that enormous time is required for enlargement of **grain size** , that bulk productivity is poor and also that it is not fitted for enlargement of area, because amorphous or monocrystal thin film is

scanned with energy beam for every **wafer** .
As described above, according to the method for forming crystal of the prior art, three...

...SPECIFICATION years for large area semiconductor devices such as solar batteries, switching transistors of liquid crystal **picture elements** , etc. in which devices are arranged in an array on an inexpensive glass.
What is...photoelectric transducing device, etc.
Also, the method of forming a polycrystalline thin film with greater **grain size** by melting and solidification has involved problems such as enormous time required for enlargement of **grain size** , poor bulk productivity and also incompatibility with enlargement of area, because amorphous or monocrystal thin film is scanned with an energy beam for every **wafer** .
As described above, according to many previous methods of forming monocrystalline material, three-dimensional integration...

20/3,K/20 (Item 20 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00310764
II-VI Group compound crystal article and process for producing the same.
Kristallisches Verbundprodukt der II-VI-Gruppe und Verfahren zu seiner Herstellung.
Produit cristallin composite du groupe II-VI et son procede de fabrication.
PATENT ASSIGNEE:
CANON KABUSHIKI KAISHA, (542361), 30-2, 3-chome, Shimomaruko, Ohta-ku Tokyo, (JP), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
Tokunaga, Hiroyuki, 10-6-402, Nanpeidai Miyamae-ku, Kawasaki-shi Kanagawa-ken, (JP)
Yonehara, Takao, 1309, Onna, Atsugi-shi Kanagawa-ken, (JP)
LEGAL REPRESENTATIVE:
Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. 2-5 Warwick Court High Holborn, London WC1R 5DJ, (GB)
PATENT (CC, No, Kind, Date): EP 284441 A2 880928 (Basic)
EP 284441 A3 891004
APPLICATION (CC, No, Date): EP 88302747 880328;
PRIORITY (CC, No, Date): JP 8771990 870326
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: **H01L-021/365** ; C23C-016/24; C30B-025/18; C23C-016/04; C23C-016/22
ABSTRACT WORD COUNT: 108

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	1200
SPEC A	(English)	EPABF1	7810
Total word count - document A			9010
Total word count - document B			0
Total word count - documents A + B			9010

INTERNATIONAL PATENT CLASS: **H01L-021/365** ...

...SPECIFICATION are arranged in an array on an inexpensive glass or switching transistors of liquid crystal **picture elements** , etc. are becoming more active year by year.

What is common in both of these...according to the prior art method has an amorphous structure or a polycrystalline structure having **grain size** distribution, and the **semiconductor** electronic element prepared in such deposited films is greatly inferior in performance as compared with a **semiconductor** electronic element prepared in a monocrystal layer. For this reason, uses are limited to simple...

...transducing element, etc.

Also, the method for forming a polycrystalline thin film with a large **grain size** by melting and solidification has the problem that enormous time is required for making **grain size** larger, because each **wafer** is scanned with an energy beam to convert an amorphous or polycrystalline thin film to a polycrystalline thin film with a large **grain size**, whereby bulk productivity is poor and the method is not suited for enlargement of areait can be formed by use of a device used in conventional **semiconductor** process, without requiring any special new preparation device.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1...monocrystal with necessary size, monocrystals shaped in a plurality of islands, a polycrystal with controlled **grain size** and **grains size** distribution, etc. can be easily formed on a base substrate of any desired material. Besides...

...is required, but it can be formed by use of a device used in conventional **semiconductor** process.

Also, the crystal according to the present invention is not restricted with respect to...

20/3,K/21 (Item 21 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00310739

III - V Group compound crystal article and process for producing the same.

Kristalliner Gegenstand aus III-V-Gruppe-Verbindung und Verfahren zu seiner Herstellung.

Article en cristal III-V et son procede de fabrication.

PATENT ASSIGNEE:

CANON KABUSHIKI KAISHA, (542361), 30-2, 3-chome, Shimomaruko, Ohta-ku Tokyo, (JP), (applicant designated states: DE;FR;GB;IT;NL)

INVENTOR:

Tokunaga, Hiroyuki, 10-6-402, Nanpeidai Miyamae-ku, Kawasaki-shi Kanagawa-ken, (JP)

Yonehara, Takao, 1309, Onna, Atsugi-shi Kanagawa-ken, (JP)

LEGAL REPRESENTATIVE:

Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. 2-5 Warwick Court High Holborn, London WC1R 5DJ, (GB)

PATENT (CC, No, Kind, Date): EP 284437 A2 880928 (Basic)
EP 284437 A3 890315

APPLICATION (CC, No, Date): EP 88302721 880325;

PRIORITY (CC, No, Date): JP 8771988 870326

DESIGNATED STATES: DE; FR; GB; IT; NL

INTERNATIONAL PATENT CLASS: **H01L-021/20** ; C30B-025/02; C30B-029/40

ABSTRACT WORD COUNT: 116

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	1169

SPEC A (English) EPABF1 7552
Total word count - document A 8721
Total word count - document B 0
Total word count - documents A + B 8721

INTERNATIONAL PATENT CLASS: **H01L-021/20** ...

...SPECIFICATION are arranged in an array on an inexpensive glass or switching transistors of liquid crystal **picture elements** , etc. are becoming more active year by year.

What is common in both of these...according to the prior art method has an amorphous structure or a polycrystalline structure having **grain size** distribution, and the **semiconductor** electronic element prepared in such deposited films is greatly inferior in performance as compared with a **semiconductor** electronic element prepared in a monocrystal layer. For this reason, uses are limited to simple...

...transducing element, etc.

Also, the method for forming a polycrystalline thin film with a large **grain size** by melting and solidification had the problem that enormous time is required for making **grain size** larger, because each **wafer** is scanned with an energy beam to convert an amorphous or polycrystalline thin film to a polycrystalline thin film with a large 1grain size , whereby bulk productivity is poor and the method is not suited for enlargement of area be formed by use of a device used in conventional **semiconductor** process, without requiring any special new preparation device.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1...monocrystal with necessary size, monocrystals shaped in a plurality of islands, a polycrystal with controlled **grain size** and **grains size** distribution, etc. can be easily formed on a base substrate of any desired material. Besides...

...is required, but it can be formed by use of a device used in conventional **semiconductor** process.

Also, the crystal according to the present invention is not restricted with respect to...

20/3,K/22 (Item 22 from file: 348)

00310736

Method of forming crystals.
Verfahren zur Herstellung von Kristallen.
Procede de preparation de cristaux.

PATENT ASSIGNEE:
CANON KABUSHIKI KAISHA, (542361), 30-2, 3-chome, Shimomaruko, Ohta-ku Tokyo, (JP), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
Yonehara, Takao, 1309 Onna, Atsugi-shi Kanagawa-ken, (JP)
LEGAL REPRESENTATIVE:
Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. 2-5 Warwick Court High Holborn, London WC1R 5DJ, (GB)

PATENT (CC, No, Kind, Date): EP 284434 A2 880928 (Basic)
EP 284434 A3 890322
APPLICATION (CC, No, Date): EP 88302718 880325;
PRIORITY (CC, No, Date): JP 8773605 870327
DESIGNATED STATES: DE; FR; GB; IT; NL

INTERNATIONAL PATENT CLASS: **H01L-021/20** ; C30B-029/06; C30B-019/12; C30B-029/06; C30B-029/40
ABSTRACT WORD COUNT: 83
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	287
SPEC A	(English)	EPABF1	6516
Total word count - document A			6803
Total word count - document B			0
Total word count - documents A + B			6803

INTERNATIONAL PATENT CLASS: **H01L-021/20** ...

...SPECIFICATION array on an inexpensive glass, such as solar batteries and switching transistors for liquid crystal **picture elements** .
What is common to these researches and developments is to require techniques by which a...converting device, etc.
Also, the method for forming a polycrystalline thin film with a large **grain size** by melting and solidification had the problem that enormous time is required for making **grain size** larger, because an amorphous or monocrystalline thin film is scanned with an energy beam for each **wafer** , whereby bulk productivity is poor and the method is not suited for enlargement of area...semiconductors such as InP, etc. capable of growth, monocrystals, monocrystal groups or polycrystals controlled in **grain size** can be formed.
Example 1
At the surface of a 5 inch Si monocrystal wafer...

...ray diffraction. As a result, it was found that 50 100 Si monocrystals having a **grain size** of 80 (mu)m with an extremely narrow distribution were formed. It was also found...

...monocrystals with necessary sizes, a plural number of island-shaped monocrystals and polycrystals controlled in **grain size** , etc. can be easily formed on the base substrate. Moreover, they can be formed by use of a device conventionally used in **semiconductor** process without requiring a special production device.
Also, the crystals of the present invention are...

20/3,K/23 (Item 23 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00310735
Crystal articles and method for forming the same
Kristalline Gegenstande und Verfahren zu ihrer Herstellung
Articles cristallins et leur procede de fabrication
PATENT ASSIGNEE:
CANON KABUSHIKI KAISHA, (542361), 30-2, 3-chome, Shimomaruko, Ohta-ku, Tokyo, (JP), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
Osada, Yoshiyuki, 1115-424, Kamiogino, Atsugi-shi Kanagawa-ken, (JP)
LEGAL REPRESENTATIVE:
Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. 2-5 Warwick Court High Holborn, London WC1R 5DJ, (GB)
PATENT (CC, No, Kind, Date): EP 284433 A2 880928 (Basic)
EP 284433 A3 890308
EP 284433 B1 981202

APPLICATION (CC, No, Date): EP 88302717 880325;
PRIORITY (CC, No, Date): JP 8773516 870327
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: **H01L-021/20** ; C30B-025/18; **H01L-021/36** ; C30B-019/12; C30B-025/02
ABSTRACT WORD COUNT: 159

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9849	547
CLAIMS B	(German)	9849	484
CLAIMS B	(French)	9849	676
SPEC B	(English)	9849	3426
Total word count - document A			0
Total word count - document B			5133
Total word count - documents A + B			5133

INTERNATIONAL PATENT CLASS: **H01L-021/20** ...

... **H01L-021/36**

...SPECIFICATION on an inexpensive glass sheet, such as solar batteries and switching transistors for liquid crystal **picture elements** .
What is common to each of these is that techniques are needed by which a...

...photoelectric transducers, etc.
Also, in the method of forming polycrystalline thin films having a large **grain size** by fusion and solidification, the amorphous or monocrystalline thin film is scanned with energy beams for each **wafer** . Accordingly, there has been a problem that the method requires much time to make the **grain size** large, it is poor in mass-productivity, and it is not suited for large area...

20/3,K/24 (Item 24 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00309737
Process for producing crystals on a light-transmissive substrate
Verfahren zur Herstellung von Kristallen auf einem Lichtdurchlassigen Substrat
Procede pour la production de cristaux sur un substrat transparent a la lumiere
PATENT ASSIGNEE:
CANON KABUSHIKI KAISHA, (542361), 30-2, 3-chome, Shimomaruko, Ohta-ku, Tokyo, (JP), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
Yonehara, Takao, 1309, Onna, Atsugi-shi Kanagawa-ken, (JP)
LEGAL REPRESENTATIVE:
Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. 2-5 Warwick Court High Holborn, London WC1R 5DJ, (GB)
PATENT (CC, No, Kind, Date): EP 289114 A2 881102 (Basic)
EP 289114 A3 890308
EP 289114 B1 980520
APPLICATION (CC, No, Date): EP 88301700 880226;
PRIORITY (CC, No, Date): JP 8747033 870302
DESIGNATED STATES: DE; FR; GB; IT; NL

INTERNATIONAL PATENT CLASS: **H01L-021/268** ; C30B-033/00; **H01L-021/20**
ABSTRACT WORD COUNT: 143

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9821	375
CLAIMS B	(German)	9821	322
CLAIMS B	(French)	9821	429
SPEC B	(English)	9821	3493
Total word count - document A			0
Total word count - document B			4619
Total word count - documents A + B			4619

INTERNATIONAL PATENT CLASS: **H01L-021/268** ...

... **H01L-021/20**

...SPECIFICATION about large area semiconductor devices such as solar batteries or switching transistors for liquid crystal **picture elements** , etc. in which elements are arranged in an array on an inexpensive glass plate are...
...P, I, and N-type layers of the PIN structure are of non-single-crystal **semiconductor** material and the effect of the light irradiation is to crystallise or recrystallise at least...

...layer in the vicinity of the boundary between it and the P or N-type **semiconductor** layer adjacent to the substrate. Where initially the I-type layer is of amorphous silicon...

...of both. If initially crystalline, the I-type layer is rendered microcrystalline of a large **grain size** (sic) or polycrystalline. In neither case is light used to reduce defects in a single...

20/3,K/25 (Item 25 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00293911
Photosensor.
Lichtsensor.
Capteur de lumiere.
PATENT ASSIGNEE:
CANON KABUSHIKI KAISHA, (542361), 30-2, 3-chome, Shimomaruko, Ohta-ku Tokyo, (JP), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
Shimada, Tetsuya, 30-1-301, Sagamigaoka, 4-chome, Zama-shi Kanagawa-ken, (JP)
Itabashi, Satoshi, 426, Onna, Atsugi-shi Kanagawa-ken, (JP)
Hatanaka, Katsunori, 7-13, Zenbu-cho Asahi-ku, Yokohama-shi Kanagawa-ken, (JP)
LEGAL REPRESENTATIVE:
Tiedtke, Harro, Dipl.-Ing. et al (11949), Patentanwalte Tiedtke-Buhling-Kinne & Partner Bavariaring 4 POB 20 24 03, W-8000 Munchen 2, (DE)
PATENT (CC, No, Kind, Date): EP 297559 A2 890104 (Basic)
EP 297559 A3 920624
APPLICATION (CC, No, Date): EP 88110403 880629;
PRIORITY (CC, No, Date): JP 87162577 870630; JP 87162578 870630; JP 87162579 870630; JP 87162581 870630

DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: **H01L-027/14** ; **H01L-021/20**
ABSTRACT WORD COUNT: 103

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	899
SPEC A	(English)	EPABF1	12986
Total word count - document A			13885
Total word count - document B			0
Total word count - documents A + B			13885

INTERNATIONAL PATENT CLASS: **H01L-027/14** ...

... **H01L-021/20**

...SPECIFICATION polishing. Therefore, as shown in Fig. 20D, single-crystal semiconductor layers 308 having a predetermined **size** are connected through the **grain** boundaries 314. The **size** of each single-crystal **semiconductor** layer 308 is determined by the distance (liters) between the nucleus formation surface micropatterns 306. By properly determining the nucleus formation micropatterns 306, the single-crystal **semiconductor** layers 308 each having a desired size can be arranged in a desired shape. Fig...response to these shift pulses.
The reference value read operation will be described below. The **image** information is output as a signal SG in response to the shift pulses CP1 and...

...are read out from the correction data memory 115 so as to correspond to the **pixels** .
The signals A0 to Am and the data Q0 to Qm are input as an...

20/3,K/26 (Item 26 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00247201
Method for forming crystalline deposited film
Verfahren zur Herstellung einer niedergeschlagenen kristalliner Schicht
Procede pour former une couche deposee cristalline
PATENT ASSIGNEE:
CANON KABUSHIKI KAISHA, (542361), 30-2, 3-chome, Shimomaruko, Ohta-ku, Tokyo, (JP), (applicant designated states: AT;BE;CH;DE;ES;FR;GB;GR;IT;LI;LU;NL;SE)
INVENTOR:
Hirai, Yutaka, 17-301, Sawa-cho 1-chome, Hikone-shi Siga-ken, (JP)
LEGAL REPRESENTATIVE:
Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. 2-5 Warwick Court High Holborn, London WC1R 5DJ, (GB)
PATENT (CC, No, Kind, Date): EP 241316 A2 871014 (Basic)
EP 241316 A3 880921
EP 241316 B1 980722
APPLICATION (CC, No, Date): EP 87303224 870413;
PRIORITY (CC, No, Date): JP 8683930 860411; JP 8785516 870406
DESIGNATED STATES: AT; BE; CH; DE; ES; FR; GB; GR; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS: **H01L-021/205** ; C23C-016/24
ABSTRACT WORD COUNT: 180

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9830	1120
CLAIMS B	(German)	9830	1044
CLAIMS B	(French)	9830	1295
SPEC B	(English)	9830	11331
Total word count - document A			0
Total word count - document B			14790
Total word count - documents A + B			14790

INTERNATIONAL PATENT CLASS: **H01L-021/205** ...

...SPECIFICATION of large area semiconductor devices such as solar batteries or switching transistors of liquid crystal **picture elements** , etc., in which devices are arranged in an array on a cheap glass are becoming...etc.

On the other hand, the method for forming a polycrystalline thin film with great **grain sizes** by melting and solidification had the problems that an enormous time is required due to scanning of amorphous or single crystal thin film with energy beam for every **wafer** to be poor in bulk productivity, and also that it is not suited for enlargement...

...if a continuous thin film may be formed, it has a polycrystalline structure with great **grain size** distribution and can be difficultly applied for **semiconductor** device.

Also, as long as a diamond substrate is used, it is expensive as a...

20/3,K/27 (Item 27 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00246800
Method for forming crystal and crystal article obtained by said method
Herstellungsverfahren eines Kristalls und so hergestellter Kristall
Methode de fabrication d'un cristal et cristal ainsi produit
PATENT ASSIGNEE:
CANON KABUSHIKI KAISHA, (542361), 30-2, 3-chome, Shimomaruko, Ohta-ku, Tokyo, (JP), (applicant designated states: AT;BE;CH;DE;ES;FR;GB;GR;IT;LI;LU;NL;SE)
INVENTOR:
Matsuyama, Jinsho, 1030-1, Yawatanakayama-cho, Nagahama-shi Shiga-ken, (JP)
Hirai, Yutaka, 301, Pares-side Jyoto 1-17, Sawa-cho, Hikone-shi Shiga-ken , (JP)
Ueki, Masao, 19-12, Higashino 3-chome, Urayasu-shi Chiba-ken, (JP)
Sakai, Akira, 1030-1, Yawatanakayama-cho, Nagahama-shi Shiga-ken, (JP)
LEGAL REPRESENTATIVE:
Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. 2-5 Warwick Court High Holborn, London WC1R 5DJ, (GB)
PATENT (CC, No, Kind, Date): EP 240309 A2 871007 (Basic)
EP 240309 A3 881005
EP 240309 B1 960828
APPLICATION (CC, No, Date): EP 87302788 870331;
PRIORITY (CC, No, Date): JP 8673093 860331; JP 8767335 870320
DESIGNATED STATES: AT; BE; CH; DE; ES; FR; GB; GR; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS: **H01L-021/20** ; C30B-025/04; C30B-023/04
ABSTRACT WORD COUNT: 87

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	1514
CLAIMS B	(English)	EPAB96	2051
CLAIMS B	(German)	EPAB96	2175
CLAIMS B	(French)	EPAB96	2218
SPEC A	(English)	EPABF1	10748
SPEC B	(English)	EPAB96	10646
Total word count - document A			12262
Total word count - document B			17090
Total word count - documents A + B			29352

INTERNATIONAL PATENT CLASS: **H01L-021/20** ...

...SPECIFICATION of large area semiconductor devices such as solar batteries or switching transistors of liquid crystal **picture elements** , etc., in which devices are arranged in an array on a cheap glass are becoming...etc.

On the other hand, the method for forming a polycrystalline thin film with great **grain sizes** by melting and solidification had the problems that an enormous time is required due to scanning of amorphous or single crystal thin film with energy beam for every **wafer** to be poor in bulk productivity, and also that it is not suited for enlargement...

...if a continuous thin film may be formed, it has a polycrystalline structure with great **grain size** distribution and can be difficultly applied for **semiconductor** device.

Also, as long as a diamond substrate is used, it is expensive as a... are flattened by selective etching of only Si, whereby a polycrystalline silicon layer controlled in **grain size** can be formed. Further, by removing the ...may be conducted before etching. When electrical field effect transistors are formed according to conventional **semi - conductor** device preparation technique on the single crystal silicon layers 15-1, 15-2 thus formed...

...or more containing no grain boundary, characteristics not inferior to that formed on single silicon **wafer** are exhibited.

Also, mutual interference between the adjacent single crystal silicon layers can be prevented...InP, etc., a single crystal, a group of single crystals or a polycrystal controlled in **grain size** and **grain size** distribution can be formed according to the present invention.

Example 1

A 5 inch Si...

...ray diffraction. As the result, it was found that 50 100 Si single crystals with **grain size** of 80 (mu)m and substantially no **grain size** distribution were formed with the above region of exposed Si(sub 3)N(sub 4...with a necessary size, a plurality of island-shaped single crystals, a polycrystal controlled in **grain size** and **grain size** distribution, etc., can be formed easily on a base substrate of any desired material. Besides...

...is required, but it can be formed by use of a device conventionally used in **semiconductor** process.

Also, the crystal according to the present invention is not limited to the materials...

...SPECIFICATION method in which melting and solidification are used to form polycrystalline thin film of large **grain size** suffers from the problems that an enormous process time is required due to the need to

scan the amorphous or single crystal thin film of every **wafer** with an energy beam, which gives poor productivity and also that the method is unsuitable...

...Even where a continuous film is formed, it has a polycrystalline structure with a large **grain size** distribution and it is difficult to use in **semiconductor** devices. Also if a diamond structure is required, the substrate is self-evidently expensive which...are flattened by selective etching of only Si, whereby a polycrystalline silicon layer controlled in **grain size** can be formed. Further, by removing the grain boundary portion, island-shaped single crystalline silicon conducted before etching. When electrical field effect transistors are formed according to conventional **semi - conductor** device preparation technique on the single crystal silicon layers 15-1, 15-2 thus formed...

...or more containing no grain boundary, characteristics not inferior to that formed on single silicon **wafer** are exhibited.

Also, mutual interference between the adjacent single crystal silicon layers can be prevented...InP, etc., a single crystal, a group of single crystals or a polycrystal controlled in **grain size** and **grain size** distribution can be formed according to the present invention.

Example 1

A 5 inch Si...

...diffraction. As the result, it was found that 50 X 100 Si single crystals with **grain size** of 80 (mu)m and substantially no **grain size** distribution were formed with the above region of exposed Si(sub(3))N(sub(4...with a necessary size, a plurality of island-shaped single crystals, a polycrystal controlled in **grain size** and **grain size** distribution, etc., can be formed easily on a base substrate of any desired material. Besides...

...is required, but it can be formed by use of a device conventionally used in **semiconductor** process.

Also, the crystal according to the present invention is not limited to the materials...

20/3,K/28 (Item 28 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

00246798

Method for forming crystalline deposited film

Herstellungsverfahren einer niedergeschlagenen Kristallschicht

Methode pour former une couche cristalline deposee

PATENT ASSIGNEE:

CANON KABUSHIKI KAISHA; (542361), 30-2, 3-chome, Shimomaruko, Ohta-ku, Tokyo, (JP), (applicant designated states: AT;BE;CH;DE;ES;FR;GB;GR;IT;LI;LU;NL;SE)

INVENTOR:

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Hirai, Yutaka, 1-17, Sawa-cho, Hikone-shi, Shiga-ken,, (JP)

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Sakai, Akira, 1030-1, Yawatanakayama-cho, Nagahama-shi, Shiga-ken,, (JP)

LEGAL REPRESENTATIVE:

Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. 2-5 Warwick Court High Holborn, London WC1R 5DJ, (GB)

PATENT (CC, No, Kind, Date): EP 241204 A2 871014 (Basic)
EP 241204 A3 881214
EP 241204 B1 960828
APPLICATION (CC, No, Date): EP 87302786 870331;
PRIORITY (CC, No, Date): JP 8673093 860331; JP 8767336 870320
DESIGNATED STATES: AT; BE; CH; DE; ES; FR; GB; GR; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS: **H01L-021/20** ; **H01L-021/205** ; C30B-025/04
ABSTRACT WORD COUNT: 168

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPAB96	697
CLAIMS B	(German)	EPAB96	642
CLAIMS B	(French)	EPAB96	708
SPEC B	(English)	EPAB96	14190
Total word count - document A			0
Total word count - document B			16237
Total word count - documents A + B			16237

INTERNATIONAL PATENT CLASS: **H01L-021/20** ...

... **H01L-021/205**

...SPECIFICATION from year to year and examples include solar batteries and switching transistors of liquid crystal **picture elements** .
A common feature of both of these techniques is the need to provide a semiconductor...method in which melting and solidification are used to form polycrystalline thin film of large **grain size** suffers from the problems that an enormous process time is required due to the need to scan the amorphous or single crystal thin film of every **wafer** with an energy beam, which gives poor productivity and also that the method is unsuitable...

...Even where a continuous film is formed, it has a polycrystalline structure with a large **grain size** distribution and it is difficult to use in **semiconductor** devices. Also if a diamond structure is required, the substrate is self-evidently expensive which...

20/3,K/29 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00820343 **Image available**
AN ACTIVE MATRIX ELECTRO-OPTIC DISPLAY
AFFICHEUR ELECTRO-OPTIQUE A MATRICE ACTIVE
Patent Applicant/Assignee:
CENTRAL RESEARCH LABORATORIES LIMITED, Dawley Road, Hayes, Middlesex UB3 1HH, GB, GB (Residence), GB (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
SURGUY Paul William Herbert, 147 Ryefield Avenue, Uxbridge, Middlesex UB10 9DA, GB, GB (Residence), GB (Nationality), (Designated only for: US)
Legal Representative:
SHARP Alan Cooper (agent), QED I.P. Services Limited, Dawley Road, Hayes, Middlesex UB3 1HH, GB,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200153887 A2-A3 20010726 (WO 0153887)

Application: WO 2001GB152 20010116 (PCT/WO GB0100152)
Priority Application: GB 20001254 20000121
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
JP US
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
Publication Language: English
Filing Language: English
Fulltext Word Count: 1799

...International Patent Class: **H01L-029/786**
Fulltext Availability:
Detailed Description

Detailed Description
... according to the invention.

Liquid crystal displays having a thin film transistor (TFT) on each **picture** **element** are well known. Analogue liquid crystal displays such as twisted nematic LCDs using cadmium selenide...

...FLC display. This is cheaper than incorporating a colour filter into the display. 11-VI **Semiconductor** materials such as CdSe or CdTe can be sputtered down as an amorphous layer at...

...is sputtered and not annealed (to keep the processing temperature low), the control of the **grain** **size** and **grain** boundaries are not good. This leads to a variation of about 0-5V in the...

20/3,K/30 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2004 WIPO/Univentio. All rts. reserv.

00816961 **Image available**
THIN-FILM TRANSISTOR AND ITS MANUFACTURING METHOD
TRANSISTOR EN COUCHES MINCES ET PROCEDE DE FABRICATION
Patent Applicant/Assignee:
SEIKO EPSON CORPORATION, 4-1, Nishishinjuku 2-chome, Shinjuku-ku, Tokyo 163-0811, JP, JP (Residence), JP (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
LUI Basil, Epson Cambridge Laboratory, 8c King's Parade, Cambridge CB2 1SJ, GB, GB (Residence), SG (Nationality), (Designated only for: US)
MIGLIORATO Piero, Epson Cambridge Laboratory, 8c King's Parade, Cambridge CB2 1SJ, GB, GB (Residence), GB (Nationality), (Designated only for: US)
YUDASAKA Ichio, Seiko Epson Corporation, 3-5 Owa 3-chome, Suwa-Shi, Nagano-Ken 392-8502, JP, JP (Residence), JP (Nationality), (Designated only for: US)
MIYASAKA Mitsutoshi, Seiko Epson Corporation, 3-5, Owa 3-chome, Suwa-shi, Nagano-Ken 392-8502, JP, JP (Residence), JP (Nationality), (Designated only for: US)
Legal Representative:
STURT Clifford Mark (agent), Miller Sturt Kenyon, 9 John Street, London WC1N 2ES, GB,
Patent and Priority Information (Country, Number, Date):

Patent: WO 200150512 A1 20010712 (WO 0150512)
Application: WO 2001GB13 20010102 (PCT/WO GB0100013)
Priority Application: GB 2000379 20000107
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 7341

Main International Patent Class: **H01L-021/336**
International Patent Class: **H01L-029/786**
Fulltext Availability:
Detailed Description

Detailed Description
... display domain 81 as shown in Fig. 5 (A). In this screen display domain 81, **pixels** are formed with data lines 90 and scan lines 91 made of metal film such as aluminum, tantalum, molybdenum, titanium, and tungsten, silicide film, and conductive semiconductor film. On each **pixel** , a liquid-crystal unit 94 (liquidcrystal cell) is formed where **image** signals are input via a TFT 30 for **image** switching. For the data line 90, a data-side driving circuit 60 is constructed that...

...88 and a level shifter 89 are constructed for the scan line 91. On each **pixel** , a retention capacitor 40 is formed connected to a c apacity line 92 running in...

...40 may be formed between a scan line 91 of the previous row and a **pixel** electrode.

As shown in Fig. 5 (B), a CMOS circuit is constructed in the data...etc.

However, in the low-teraperature process, because it is difficult to form a polycrystalline **semiconductor** film of high crystallinity directly on the substrate, first of all an amorphous **semiconductor** 100 needs to be formed using the plasma CVD method or the lowpressure CVD method, and then this **semiconductor** film 100 needs to be crystallized as is explained below. As the method of this...

...Crystallization Process) is used, temperature increase of the substrate can be suppressed and a large- **grain** - **size** polycrystalline **semiconductor** film can be obtained.

In this cr
, ystallization process, a laser beam (excimer laser) emitted...
?

22/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00962831

Methods of forming integrated circuit capacitors having improved electrode and dielectric layer characteristics and capacitors formed thereby

Herstellungsverfahren von Kondensatoren fur integrierte Schaltungen mit verbesserten Charakteristiken von Elektroden- und Dielektricumschichten sowie so hergestllete Kondensatoren

Procede de fabrication de condensateurs pour circuits integres ayant des caracteristiques ameliorees d'electrode et de dielectrique et condensateurs ainsi obtenus

PATENT ASSIGNEE:
Samsung Electronics Co., Ltd., (2171361), 416 Maetan-dong, Paldal-gu, Suwon City, Kyungki-do, (KR), (Applicant designated States: all)
INVENTOR:
Kim, Young-Sun, 20-33 Gongduk-Dong, Mapo-Gu, Seoul, (KR)
Won, Seok-Jun, No. 1603-25, Bongcheon 7-dong, Kwanak-gu, Seoul, (KR)
Kim, Young-Min, No. 380 Kugal-ri, Kiheung-eup, Yongin-city, Kyungki-do, (KR)
Kim, Kyung-Hoon, No. 31-4, Wonhyoro 1-ga, Yongsan-gu, Seoul, (KR)
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Lee, Seung-Hwan, 817-7, Bangbae-Dong, Seocho-Gu, Seoul, (KR)
Lee, Sang-Hyeop, No. 1403-B-Marronnier-dong,7-1 Nongseo-li,, Kihung-up,Yongsin-shi,Kyunggi-do,, (KR)
Shim, Se-Jin, 1804-503 Haetbit-maeul, Dukyang-gu, Koyang-shi, Kyunggi-do, (KR)
Jin, You Chan, 101-801, Woosung Apt, Maetan-Dong, Paldal-Gu, Suwon-City, Kyunggi-Do, (KR)
Moon, Ju-Tae, 1309 Youngkwang-APT, Songjuk-dong, Jangan-gu, Suwon-shi, Kyunggi-do, (KR)
Choi, Jin-Seok, 104-202, Hankiik Apt, Maetan-Dong, Paldal-Gu, Suwon-City, Kyunggi-Do, (KR)
LEGAL REPRESENTATIVE:
Tunstall, Christopher Stephen (72841), Harrison Goddard Foote, Fountain Precinct, Leopold Street, Sheffield·S1 2QD, (GB)

PATENT (CC, No, Kind, Date): EP 874393 A2 981028 (Basic)
EP 874393 A3 011205
APPLICATION (CC, No, Date): EP 98302397 980327;
PRIORITY (CC, No, Date): KR 9735460 970728; KR 9748930 970926; KR 9714833 970422; KR 9723381 970605; KR 9716812 970430
DESIGNATED STATES: DE; FR; GB; IT; NL
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: H01L-021/3205; H01L-021/02
ABSTRACT WORD COUNT: 211
NOTE:
Figure number on first page: 1B

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9844	2240
SPEC A	(English)	9844	7047
Total word count - document A			9287

Total word count - document B 0
Total word count - documents A + B 9287

...ABSTRACT A2
Methods of forming **integrated circuit** capacitors include the steps of forming a lower electrode of a capacitor by forming a conductive layer pattern (e.g., silicon layer) on a **semiconductor** substrate and then forming a hemispherical grain (HSG) silicon surface layer of first conductivity type...
...layer pattern increases the effective surface area of the lower electrode for a given lateral **dimension** . The **HSG** silicon surface layer is also preferably sufficiently doped with first conductivity type dopants (e.g...

...SPECIFICATION capacitors having HSG surface layers therein (hereinafter "HSG capacitors") have manifested enhanced capacitance in high **density** **integrated circuits** , **HSG** capacitors may lack stability and may incur performance degradation over the lifetime of an **integrated circuit** memory device. Studies have shown that the capacitance of a conventional HSG capacitor can vary...

...layer pattern increases the effective surface area of the lower electrode for a given lateral **dimension** . The **HSG** silicon surface layer is also preferably sufficiently doped with first conductivity type dopants (e.g...

22/3,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00662860
Spin-on conductor process for integrated circuits.
Verfahren, um Leiter durch "Spin-on"-Verfahren fur integrierte Schaltungen aufzutragen.
Procede pour deposer un conducteur par "Spin-on" pour circuits integres.
PATENT ASSIGNEE:
AT&T GLOBAL INFORMATION SOLUTIONS INTERNATIONAL INC., (1449481), 1700 South Patterson Boulevard, Dayton, Ohio 45479, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
Allman, Derryl D.J., 2825 Zephyr Drive, Colorado Springs, CO 80920, (US)
Lee, Steven S., 3813 Clovergate Drive, Colorado Springs, CO 80920, (US)
LEGAL REPRESENTATIVE:
Gill, David Alan et al (69772), W.P. Thompson & Co., Celcon House, 289-293 High Holborn, London WC1V 7HU, (GB)
PATENT (CC, No, Kind, Date): EP 637072 A2 950201 (Basic)
EP 637072 A3 950503
APPLICATION (CC, No, Date): EP 94305496 940726;
PRIORITY (CC, No, Date): US 96810 930726
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: H01L-021/768; H01L-021/3205;
ABSTRACT WORD COUNT: 132

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF2	249
SPEC A	(English)	EPABF2	3829
Total word count - document A			4078

Total word count - document B 0
Total word count - documents A + B 4078

...SPECIFICATION etch is required to remove the majority of the tungsten from the surface of the **wafer** . Second, when the tungsten is removed from the surface, the barrier material is exposed at...

...leave a void. The third disadvantage arises from the fact that tungsten is deposited by **grain growth** , and the final tungsten film is composed of individual merged grains. Gaseous tungsten may be...

22/3,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00570612
Semiconductor device including a wiring layer
Halbleiteranordnung mit einer Leiterschicht
Dispositif semi-conducteur comprenant une couche conductrice
PATENT ASSIGNEE:
Samsung Electronics Co., Ltd., (2171367), San 24 Nongseo-ri Kiheung-eub, Yongin-city Kyungki-do, (KR), (applicant designated states: DE;FR;GB;IT)
INVENTOR:
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Park, Chang-Soo, 1-101, Woojoo Town, 167, Maetan 1-Dong, Kwonsun-ku, Suwon, Kyungki-Do, (KR)
LEGAL REPRESENTATIVE:
Finnie, Peter John et al (79522), Elkington and Fife, Prospect House, 8 Pembroke Road, Sevenoaks, Kent TN13 1XR, (GB)
PATENT (CC, No, Kind, Date): EP 552968 A2 930728 (Basic)
EP 552968 A3 930929
EP 552968 B1 981125
APPLICATION (CC, No, Date): EP 93300459 930122;
PRIORITY (CC, No, Date): KR 90492 920123
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: H01L-023/485; H01L-021/60; H01L-021/768;
ABSTRACT WORD COUNT: 202

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9848	1310
CLAIMS B	(German)	9848	1270
CLAIMS B	(French)	9848	1539
SPEC B	(English)	9848	9737

Total word count - document A 0
Total word count - document B 13856
Total word count - documents A + B 13856

...SPECIFICATION to this patent, a predetermined first thickness of a metal layer is deposited on a **semiconductor wafer** at a cold temperature. Then, the temperature is increased to approximately 400(degree)C to...

...second thickness of the metal layer. The reflow of the metal layer takes place through **grain growth** , recrystallization and bulk diffusion. According to the Tracy et al. method, the step coverage of...of about 6,000A at a room temperature, the metal layer thus obtained has a **grain size** as small as 0.2(mu)m. Thus, the step coverage of a sputtered Al...

22/3,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00279239
FABRICATION OF SOLID-STATE DEVICES HAVING THIN DIELECTRIC LAYERS.
VERFAHREN ZUR HERSTELLUNG VON FESTKORPERN EINRICHTUNGEN MIT DUENNEN DIALEKTRISCHEN SCHICHTEN.
FABRICATION DE DISPOSITIFS A SEMI-CONDUCTEURS AYANT DES COUCHES DIELECTRIQUES MINCES.
PATENT ASSIGNEE:
AMERICAN TELEPHONE AND TELEGRAPH COMPANY, (589370), 550 Madison Avenue, New York, NY 10022, (US), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
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MAURY, Alvaro, 5906 Club House Lane, Wescosville, PA 18106, (US)
STINEBAUGH William, Henry, Jr., 1907 Homestead Avenue, Bethlehem, PA 18018, (US)
LEGAL REPRESENTATIVE:
Johnston, Kenneth Graham et al (32382), AT&T (UK) LTD. AT&T Intellectual Property Division 5 Mornington Road, Woodford Green Essex, IG8 OTU, (GB)
PATENT (CC, No, Kind, Date): EP 258394 A1 880309 (Basic)
EP 258394 B1 930602
WO 8705152 870827
APPLICATION (CC, No, Date): EP 87901849 870206; WO 87US272 870206
PRIORITY (CC, No, Date): US 833884 860225
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: H01L-021/28; H01L-021/316;
NOTE:
No A-document published by EPO
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	284
CLAIMS B	(German)	EPBBF1	277
CLAIMS B	(French)	EPBBF1	318
SPEC B	(English)	EPBBF1	1821
Total word count - document A			0
Total word count - document B			2700
Total word count - documents A + B			2700

...SPECIFICATION of the amorphouse silicon to polysilicon. Application of the present technique to the production of **integrated circuits** and other solid state devices is possible. Silicon is considered to be amorphous when only short-range order is present at the atomic level, with any resulting **grains** having a **size** of less than 1 nanometer, as determined by x-ray or electron diffraction techniques known...

22/3,K/5 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

01154922 **Image available**
CRYSTALLIZATION APPARATUS AND METHOD OF AMORPHOUS SILICON
SYSTEME ET PROCEDE DE CRISTALLISATION DE SILICIUM
Patent Applicant/Assignee:

SAMSUNG ELECTRONICS CO LTD, 416, Maetan-dong, Yeongtong-gu, 442-742 Suwon-si, Gyeonggi-do, KR, KR (Residence), KR (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
CHUNG Ui-Jin, Jookong Greenville Apt. 103-104, 1258, Maetan 3-dong, Paldal-gu, 442-804 Suwon-si, Gyeonggi-do, KR, KR (Residence), KR (Nationality), (Designated only for: US)
KIM Dong-Byum, Hyundai Villa 403, 43-1, Cheongdam-dong, Kangnam-ku, 135-100 Seoul, KR, KR (Residence), KR (Nationality), (Designated only for: US)
LEE Su-Gyeong, 202, 1546-10, Shinlim 9-dong, Kwanak-ku, 151-860 Seoul, KR , KR (Residence), KR (Nationality), (Designated only for: US)
KANG Myung-Koo, Misung Apt. 3-205, Shincheon-dong, Songpa-ku, 133-240 Seoul, KR, KR (Residence), KR (Nationality), (Designated only for: US)
KIM Hyun-Jae, Chunggu Apt. 601-903, 123, Imae-dong, Bundang-ku, 463-830 Seongnam-si, Gyeonggi-do, KR, KR (Residence), KR (Nationality), (Designated only for: US)
Legal Representative:
YOUME PATENT AND LAW FIRM (agent), Teheran Bldg., 825-33, Yoksam-dong, Kangnam-ku, Seoul 135-080, KR,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200477544 A1 20040910 (WO 0477544)
Application: WO 2004KR382 20040224 (PCT/WO KR04000382)
Priority Application: KR 1020030011643 20030225
Designated States:
(All protection types applied unless otherwise stated - for applications 2004+)
AE AG AL AM AT AU AZ BA BB BG BR BW BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NA NI NO NZ OM PG PH PL PT RO RU SC SD SE SG SK SL SY TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT RO SE SI SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) BW GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 5315
Fulltext Availability:
Detailed Description

Detailed Description
... the laser beam 1 th rough the slit 61 11 in the previous shot. The **grain growth** in the lower half of the regio ns in this shot starts from a boundary...

...in the p revious shot and proceeds in the upward direction, which is the same **growing** direction of the **grain** . As a result, the grain formed in the previous shot extends to the upward di...

22/3,K/6 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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01044043
IMPROVED CHEMICAL-MECHANICAL POLISHING SLURRY FOR POLISHING OF COPPER OR SILVER FILMS
PATE DE POLISSAGE MECANO-CHIMIQUE AMELIOREE, UTILISEE DANS LE POLISSAGE DE FILMS DE CUIVRE OU D'ARGENT

Patent Applicant/Assignee:
UNIVERSITY OF FLORIDA, P.O. Box 115500, Gainesville, FL 32611-5500, US, US (Residence), US (Nationality)
Inventor(s):
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LEE Seung-Mahn, 4440 Archer Road #427, Gainesville, FL 32608, US,
Legal Representative:
NELSON Gregory A (agent), Akerman, Senterfitt, Post Office BOx 3188, West Palm Beach, FL 33402-3188, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200372670 A1 20030904 (WO 0372670)
Application: WO 2003US2618 20030129 (PCT/WO US0302618)
Priority Application: US 200281979 20020222
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SC SD SE SG SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT SE SI SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 14871

Fulltext Availability:
Detailed Description

Detailed Description
.... Example 14; The use of Halide Chemistries on the Polishina of Silver.

1 5 A **wafer** coated with a silver layer was dipped in a 10 mN iodine solution at a...
...EDX data showing the formation of a silver iodide layer after dipping a silver coated **wafer** in the
48
iodine containing slurry. A thin continuous layer is formed at the surface as shown in each of the SEMs. The **grain** **size** is about 0.4 microns, or less. The AgI layer can be seen to entirely...